TM 9-4935-483-34

TECHNICAL MANUAL

DS AND GS MAINTENANCE MANUAL

TEST SET, GUIDED MISSILE INFRARED TRACKER

AN/TSM 114

This copy is a reprint which includes current pages from Changes 1 and 2.

HEADQUARTERS, DEPARTMENT OF THE ARMY
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HEADQUARTERS,
DEPARTMENT OF THE ARMY
Washington, D. C., *4 April 1977*

DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL
TEST SET, GUIDED MISSILE INFRARED TRACKER
AN/TSM 114

LIST OF ILLUSTRATIONS

PART NUMBER CONFIGURATION STATUS TABLE

This table is provided to enable maintenance personnel to determine if all authorized configuration changes have been incorporated inthe equipment. The table is organized in figure number sequence as arranged int his manual. Beside each equipment item listed you will find the part number history of the item. The latest part number will be listed first with previous part numbers following in descending order. After the part number history is a list of all applicable Modification Instuctions (MI's) pertaining to the item. Mainetance personnel are urged to constantly refer to this table in order to keep their equipment up-to-date. Part numbers will be removed from the schematic diagrams by future manual changes. Therefore, the part number configuration status table will become your source for the latest part number information.

When manual change pages are published as a result of approved configuration changes, the TM change transmittal sheet will indicate the applicable MI(s) and the affected pages. Be sure to retain the old pages until the modification has been applied to all of your equipment then insert the new change pages.

FIG.NO.	ITEM	PART NO. HISTORY	APPICABLE MI'S
1-1	Test Set Guided Missile Infrared Tracker-AN/TSM 114.	10277970	' ' ' ' '
2-23	Optical Alignment Fixture	10277942	' ' ' '
2-24	OAC Optical Functions	10220300	----
2-25	Monitor Unit	10277941	------
2-26	Electronic Component Assembly 1A1A1	10276959/10219959	' ' ' '
2-27	Circuit Card Assembly 1A1A2	10276593/102783510	MI 07461A-40/1
2-28	Circuit Card Assembly 1A1A3	10278354	----
2-29	Circuit Card Assembly 1A1A4	10277931	-----
2-30	Circuit Card Assembly 1A1A5	10277934	----
2-31	Circuit Card Assembly 1A1A6	10277929	------
2-32	Circuit Card Assembly 1A1A7	10277935	-----
2-33	Circuit Card Assembly 1A1A8	10278379	------
2-34	Circuit Card Assembly 1A1A9	10278384	------
2-35	Circuit Card Assembly 1A1A10	10278326	----

FIG. NO.	ITEM	PART NO. HISTORY	APPLICABLE MI'S
2-36	Electronic Component Assembly 1A1A11	10276958/10278393	----
2-38	Circuit Card Assembly 1A2A1	10277940	----
2-39	Optical Alignment Collimator	10220300	----
2-39	Circuit Card Assembly 1A3A1	10220296	----
2-40	Circuit Card Assembly 1A4A1	10278213	----
3-2	Circuit Card Assembly 1A1A2A1	10278352	----
3-3	Circuit Card Assembly 1A1A2A2	10220043	----
3-3	Circuit Card Assembly 1A1A2A2A1	10276592/10278311	----
3-4	Circuit Card Assembly 1A1A3A1	10278355	----
3-5	Circuit Card Assembly 1A1A3A2	10220049	----
3-6	Circuit Card Assembly 1A1A4A1	10220054	----
3-7	Circuit Card Assembly 1A1A4A2	10278362	----
3-8	Circuit Card Assembly 1A1A5A1	10278365	----
3-9	Circuit Card Assembly 1A1A5A2	10277937	----
3-10	Circuit Card Assembly 1A1A6A1	10277925	----
3-11	Circuit Card Assembly 1A1A6A2	10277927	----
3-12	Circuit Card Assembly 1A1A7A1	10278375	----
3-13	Circuit Card Assembly 1A1A7A2	10277936	----
3-14	Circuit Card Assembly 1A1A8A1	10278382	----
3-15	Circuit Card Assembly 1A1A8A2	10278380	----
3-16	Circuit Card Assembly 1A1A9A1	10278385	----
3-17	Circuit Card Assembly 1A1A9A2	10278387	----
3-18	Circuit Card Assembly 1A1A1OA1	10220090	----
3-19	Circuit Card Assembly 1A1A10A2	10278327	----
3-20	Circuit Card Assembly 1A1A11A1	10278394	----
4-1	Optical Alignment Fixture Base - Disassembly and Assembly	10278309	----

SAFETY SUMMARY

The following are general safety precautions that personnel must understand and apply during operation and maintenance.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must observe safety regulations at all times. Do not replace components or make adjustments inside the equipment with high voltage present. Under certain conditions, dangerous potentials may exist when the power control is in the off position. To avoid injury, remove power and discharge and ground a circuit before touching it.

DO NOT SERVICE OR ADJUST ALONE

Under no circumstances should any person reach into the enclosure for the purpose of servicing or adjusting the equipment except in the presence of someone who is capable of rendering aid.

RESUSCITATION

Personnel working with or near high voltages should be familiar with modern methods of resuscitation.

CHAPTER 1
INTRODUCTION

Section I. GENERAL

1-1. Purpose and Scope.

This manual contains a description of, and instructions for, the direct support and general support maintenance of the Test Set, Guided Missile Infrared Tracker, AN/TSM 114, (fig. 1-1). It is to be used in conjunction with TM 9-4935-480-14. Hereafter in this manual the Tracker Test Set will be identified as the TTS.

1-2. Troubleshooting Procedures.

Troubleshooting and testing of the TTS and subassemblies will be accomplished by the procedures contained in chapter 3.

1-3. Forms, Records, and Reports.

All personnel and organizations responsible for operating and/or maintaining this equipment are also responsible for the preparation and disposition of appropriate forms, records, and reports.

1-4. Security Responsibilities.

a. The security classification of the DRAGON Weapon System Equipment is UNCLASSIFIED. Portions of data relative to the DRAGON system are classified.

b. The importance of security of classified material cannot be overemphasized. Security is an individual, as well as a command, responsibility.

c. Installation security and safeguarding of classified material will be in accordance with current directives.

1-5. Reports of Equipment Manual Improvements.

Reports of errors, omissions, and recommendations for improving this publication by the individual user are encouraged. U. S. Marine Corps reports should be submitted on Form NAVMC 10772 in accordance with MCO 5600.41 . All others should be submitted on DA Form 2028, Recomnended Changes to Publications, and forward directly to: Commander, U. S. Army Missile Command, ATTN: DRSMI-NPMS, Redstone Arsenal, Alabama 35809.

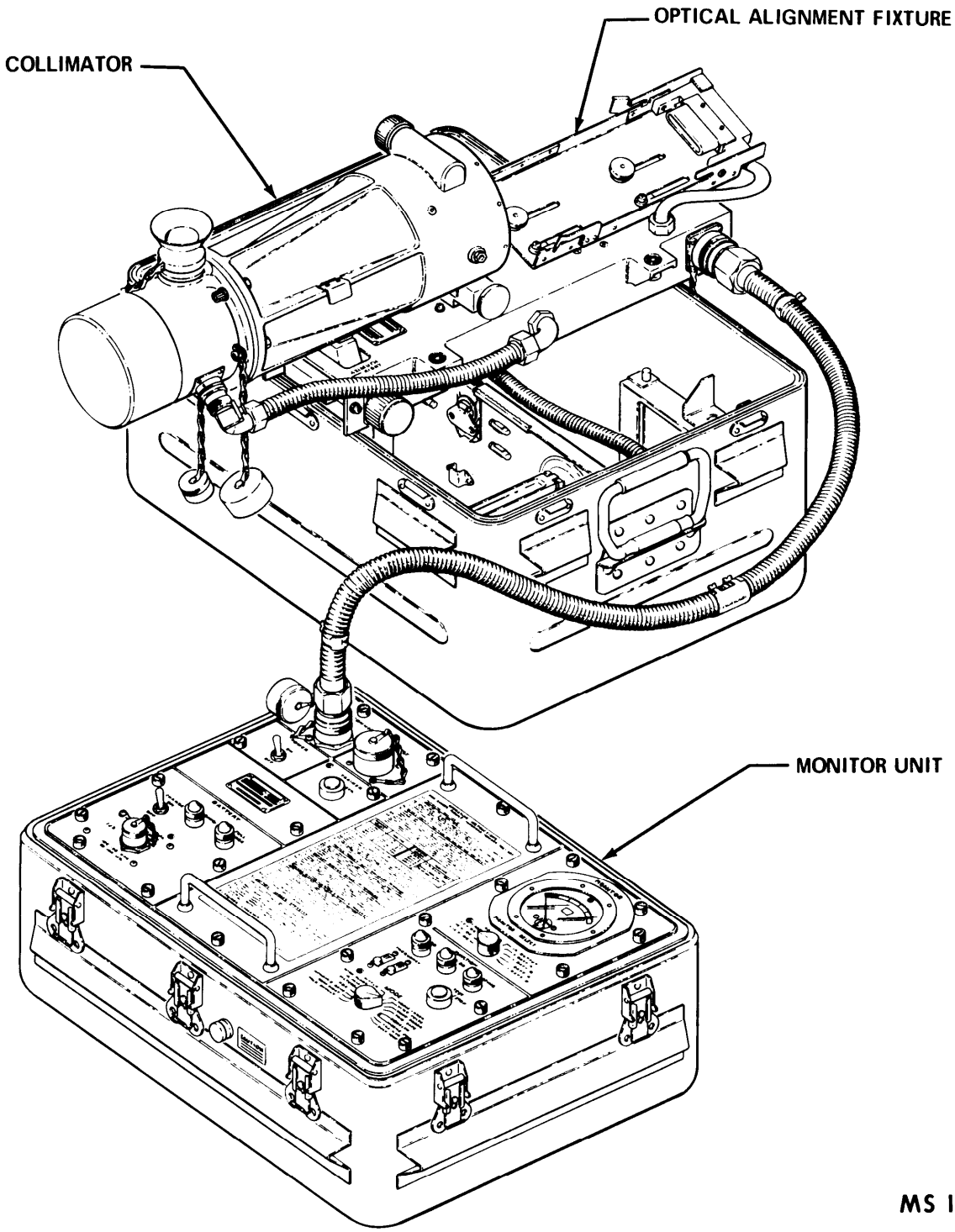

Figure 1-1. Test set guided missile infrared tracker, AN/TSM 114 (10277930)

1-6. Shipment and Storage.

Data related to the shipment and storage of the TTS are contained in TM 9-4935-480-14.

Section II. DESCRIPTION AND DATA

1-7. Physical Description.

a. The TTS is a crew portable, battery operated, test set designed for field use with the DRAGON system. The TTS tests the Infrared Tracker, GM, SU-36/P, Launch Effects Trainer, GM, M54 and Monitoring Set, GM, Training, AN/TSQ-T1.

b. The TTS is composed of three major subassemblies as depicted in figure 1-1.

(1) The optical alignment fixture (OAF) is a channeled metal platform for mounting the tracker. It has mechanical provisions for mounting and aligning the infrared visual alignment collimator, hereafter called the (OAC) with reference to the tracker. The OAF electrically interconnects the monitor unit with the OAC and the tracker. It also houses printed circuit card 2A1. The OAF has light intensity controls used during self-test and testing. The OAF is stored in the case cover and is rigidly mounted on the inverted cover during testing.

(2) The OAC is a cylindrical metal object, housing an objective lens assembly, a collimator reticle assembly, an eyepiece assembly, an electronics assembly (printed circuit card 3A1), and the infrared (IR) diodes utilized to stimulate the tracker during test. The objective lens is used to focus the IR source onto the detector assembly of the tracker, and is adjusted by a mechanical knob located on the top forward end of the OAC. The reticle cell contains a reticle with five aim points and horizontal and vertical crosshairs graduated in milliradians. The eye-piece assembly presents the reticle to the operator and is adjusted by a focusing ring to adapt the optics to the individual operator’s eyesight. The two IR diodes, a self-test light, and a reticle backlight are located in the aft end of the OAC.

(3) The monitor unit contains the unit power system, stimuli electronics, monitoring electronics, and a control panel.

c. Complete physical data and further description of the TTS are contained in TM 9-4935-480-14.

1-8. Functional Description.

a. The TTS is used to provide operational go or no go checks of the DRAGON tracker and, if the tracker is defective, to identify the failed test mode. Go or

no go checks of the tracker is accomplished by stimulating the tracker detector assembly with an IR source modulated at known frequencies, and evaluating the electrical outputs of the tracker. It also checks the output of the tracker firing mechanism. The TTS provides the capability for an operational evaluation, by the operator, of the launch effects trainer (LET) and the trainer monitoring set (MTS).

b. The TTS has self-test capabilities, which provide a check of the test set batteries, voltage regulators, and IR source. When operating on fully charged batteries with no external power applied, it can check approximately 14 trackers and perform four self tests without battery recharging.

Section III. DEMOLITION TO PREVENT ENEMY USE

1-9. Methods of Destruction.

If capture or abandonment of the TTS to an enemy is imminent, the responsible unit commander may decide to destroy it. Based on this decision, the TTS may be rendered inoperable by one of the following means:

a. Placing 1/2 pound of composition explosive in direct contact with the piece to be destroyed and detonating with a safety fuse.

b. Weapon fire.

c. Manually smashing with any available heavy object.

d. Disassembly, scattering and concealment.

1-10. Items to be Destroyed.

When the TTS is to be destroyed, regardless of method, the following priority should be used:

a. Optical alignment collimator.

b. Monitor unit.

c. Optical alignment fixture.

CHAPTER 2
THEORY OF OPERATION

2-1. Operational Description.

a. The TTS overall block diagram (fig. 2-1) depicts overall operation of the test set. When it is connected to an ac source, power is applied to the battery charger circuits through a stepdown transformer; this will maintain the battery pack in a full charge condition. Output of the battery pack is fed to the regulators. The regulators provide operating voltages for the monitor unit, OAF, OAC, and tracker. A simulated tracker load is used during self test. The tracker is mounted on the OAF and interfaced through a 15-pin connector. The OAF contains the lamp illumination controls for the OAC testing lights. Card 2A1, located in the OAF, contains the IR source current control generator. The tracker is stimulated by the IR energy emitted through the OAC lens. This IR energy is generated by the IR source diodes CR1 and CR2 located in the OAC. These diodes are stimulated by the IR signal generator, card 1A8 (monitor unit), and card 2A1 (OAF). Frequency and level of the applied IR signal is determined by the position of mode switch S6 and setting of the frequency switch. The OAC also contains IR detector CR3 (along with card 3A1), used in self-test mode for detection of the OAC IR output. Card 1A3 provides a simulated first motion discrete signal to the tracker to provide a start signal to the tracker circuits for program evaluation. Card 1A3 also provides a frequency select to the tracker and a cam solenoid inhibit signal (CSI) which drives the K1 relay in the OAF for operation in trainer and boresight modes. The relay then applies +13 Vdc to the tracker. Master clock card 1A4 is used for the generation of the evaluation testing gates.

b. Evaluation of the tracker (UUT) is performed by the following TTS cards; (fig. 2-1) filters, cards 1A10; wire clamps, cards 1A5 and 1A6; ripple, card 1A6; horizontal error, cards 1A6; vertical pulse, card 1A5; vertical error, cards 1A5; trigger safe, card 1A7; squelch, cards 1A5, 1A6 and 1A10; IR pulse, cards 1A8, and 1A10; dynamic gain, cards 1A3 and 1A9; AGC, card 1A10; trigger output, card 1A7. Cards 1A10, 1A7, and 1A6 also contain the composite logic for determination of go or no-go status. The cards provide input to testing, go and no-go lamp drivers on card 1A3 for illumination of these indicators. Card 1A10 provides a simulated sum signal for use in testing the trainer monitoring set (MTS). Card 1A8 provides a simulated trigger pulse to the Launch Effects Trainer (LET). Card 1A8 contains the

training frequency decode circuit providing training frequency stimulus to the UUT during operation in the trainer and boresight modes.

c. The TTS has five major modes of operation: (fig. 2-1) self-test, trigger output, boresight, missile command, and trainer. No power is delivered to the collimator reticle light, self-test light, and tracker reticle light in the OAF during periods of operation in a major test mode. A description of each mode of operation is presented in the following paragraphs.

(1) The self-test mode verifies the operation of the three function indicators and the ability of the battery packs and voltage regulators to supply the proper voltages to the TTS under simulated load conditions. When the test start/stop switch is depressed, the battery packs supply currents to R1 and R2 on card 1A2. These resistors present a simulated load to the TTS. During self-test, no power is applied to the UUT. This permits testing of the TTS with or without a UUT installed. The three function indicators illuminate for the duration of the self-test. All lamps are illuminated by the testing logic and lamp drivers on card 1A3. The monitor select switch is rotated by the operator for the presentation on the monitor meter of the desired measurements. During self-test, IR emitting diode CR1 in the OAC is stimulated at both high and low intensity levels. Photodetector diode CR3 receives the IR signal from CR1. This signal is amplified by card 3A1 in the OAC, conditioned by card 1A9 in the monitor unit, and then coupled to the monitor meter when the monitor select switch is in the IR output position. If this signal is of the proper level, the meter will read in the green area of the IR output scale. All other readings on the meter are made on the 0 to 15 voltage scale.

NOTE

With fully charged batteries, the meter may read off-scale to the right on the +13 Vdc and -13 Vdc positions of the monitor select switch. This is an acceptable condition.

(2) The trigger output mode verifies that the output signal of the UUT firing mechanism is an energy pulse of 17 mil joules ± 7 percent for a maximum time duration of 10 msec when fired into a 1.25 ohm load. No power is applied to the UUT in this mode of operation. After the test start/stop switch is depressed, the UUT firing mechanism is manually fired by the test set operator, applying a pulse to the evaluation card 1A7. The testing indicator will illuminate upon depression of the test start/stop switch and will extinguish where either the go or no-go

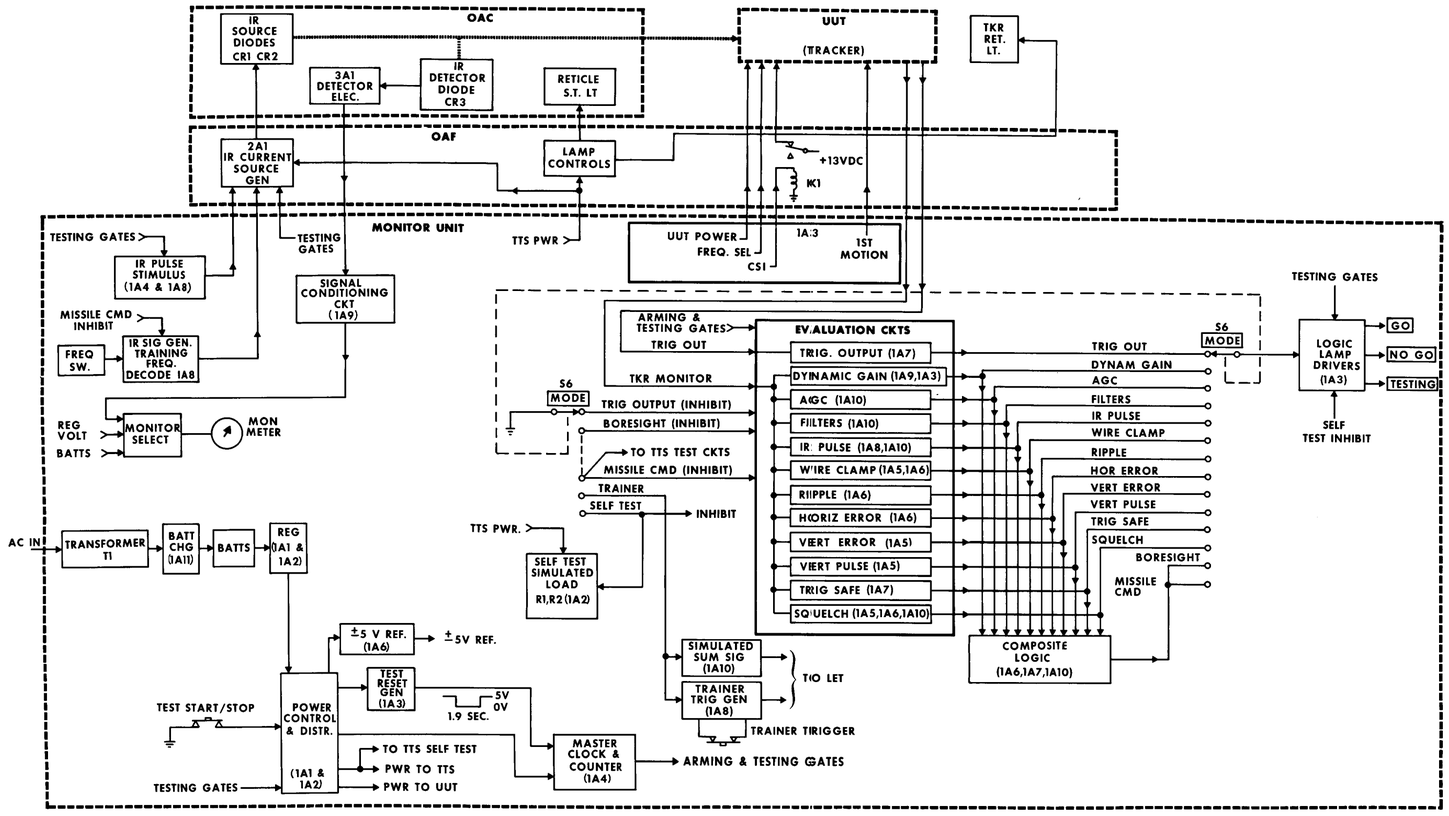

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Figure 2-1 Tracker test set-functional block diagram

indicator illuminates. The go indicator will illuminate immediately upon UUT firing mechanism activation if the energy is within the allowable parameters. The no-go indicator will illuminate at Ts +21 seconds for a rejected pulse. The indicators extinguish at Ts +30 seconds.

(3) The boresight test is performed with the OAC IR source aligned with the center of the UUT detector assembly, simulating a line-of-sight missile trajectory. This test evaluates the response of the UUT to this stimuli. The IR source, CR1 near-center diode, is modulated at the training frequency in this mode of operation. At Ts +19 seconds through Ts +20 seconds, CR2 (off-center diode) is activated, which simulates a missile shift from line of sight (boresight) to right 17.8 MR and up 4.45 MR.

(a) When the teststart/stop switch is depressed and released, the power-on relay (1A1) is energized. The battery packs deliver, via the power relay contacts, ±20 Vdc to the ±13 Vdc regulators (1A2), the ±5.0 Vdc reference (1A6), and the +5.0 Vdc digital (1A1) voltage regulators. The regulators' output energizes the UUT power relay (1A2) and the test set evaluation circuits, and initiates the reset function. The reset function lasts for 1.9 seconds. During this period, all UUT and test set functions are brought to zero reference. At the end of the 1.9 seconds the reset is released, which constitutes Ts. In this mode, at Ts, the UUT power relay applies power to the UUT and enables the first motion discrete circuit, the cam solenoid inhibit circuit, and the frequency select circuit of card 1A3. The TTS will automatically program through a test cycle, varying the stimuli to the UUT, and evaluate the UUT outputs.

(b) At Ts +20 seconds, power is removed from the UUT. The testing indicator, which illuminated at Ts, will extinguish at Ts +21 seconds. At the same times the composite gate logic circuits are enabled, allowing go or no-go decision to illuminate the proper function indicator. If the go indicator illuminates, testing power will remain on until Ts +30 seconds. If the no-go indicator illuminates, testing power will remain on until Ts +60 seconds, allowing time for the operator to rotate the mode switch for an identification of the failed UUT parameter. The status of each tested parameter will be indicated on the go or no-go indicator as the mode switch is rotated. The tests performed in this mode are: dynamic gain, AGC, filters, wire clamps, ripple, horizontal error, vertical pulse, vertical error, and trigger safe.

(4) The missile command mode of operation is similar to the boresight mode, except the OAC IR source is supplied from the near-center diode CR1 and the OAC is

mechanically repositioned to simulate a target 2.36 MR left and 2.36 MR down off of boresight. This is done by mechanically repositioning the OAC. During this mode of operation, the off-center diode CR2 is not activated.

(a) The tactical frequency is selected in this mode of operation via the frequency selector digit switch. The frequency selector output is coupled to card 1A8 for decoding and generation of the IR source stimuli. The stimuli is generated by the high frequency crystal oscillator in card 1A8. The oscillator generates three frequencies which are decoded and used to generate a center frequency source and a high and low frequency source. This signal is used to modulate the IR source current generator on card 2A1. From Ts seconds until Ts +13 seconds, the IR diode CR1 is modulated at center tactical frequency. From Ts +13 seconds until Ts +14.5 seconds, the frequency is shifted above the center frequency. From Ts +14.5 seconds until Ts +16 seconds, the frequency is shifted below the tactical center frequency. At Ts +16 seconds, the frequency is shifted again to center where it remains for the duration of the test cycle. Purpose of this frequency shift is to test the band-pass filter of the UUT.

(b) This results in a IR pulse imposed on the normal sinusoidal modulated IR signal being fed out of the OAC and into the UUT detector. This is called an IR false sample test and is performed to evaluate the UUT AGC clamp capability. During Ts +10 seconds through Ts +11 seconds, the near-center diode CR1 is modulated by the IR source control voltage (1.77 VRMS sine wave) which has a 20 usec (PW) 100 Hz square wave pulse superimposed on it from monitor card 1A8 and 1A4.

(c) The TTS will evaluate the UUT response to the stimuli and provide an indication similar to that described for the boresight mode. The UUT parameters evaluated in the missile command mode are: filters, IR pulse, wire clamps, ripple, horizontal error, vertical pulse, vertical error, trigger safe, and squelch.

(5) The trainer mode of operation (fig. 2-2) provides the means for an operational evaluation of the LET and MTS. An operational tested go UUT is mounted on the OAF in the same manner as if undergoing testing. The trainer adapter of the TTS provides the means for interconnection of the TTS, LET and MTS. The cabling is as shown in TM 9-4935-480-14. The TTS, in the trainer mode, provides three functions to the UUT, LET and MTS.

(a) The TTS provides an IR stimuli to the UUT. This stimuli comes from card 1A8 through the OAC and utilizes the same circuits provided for boresight and missile command tests.

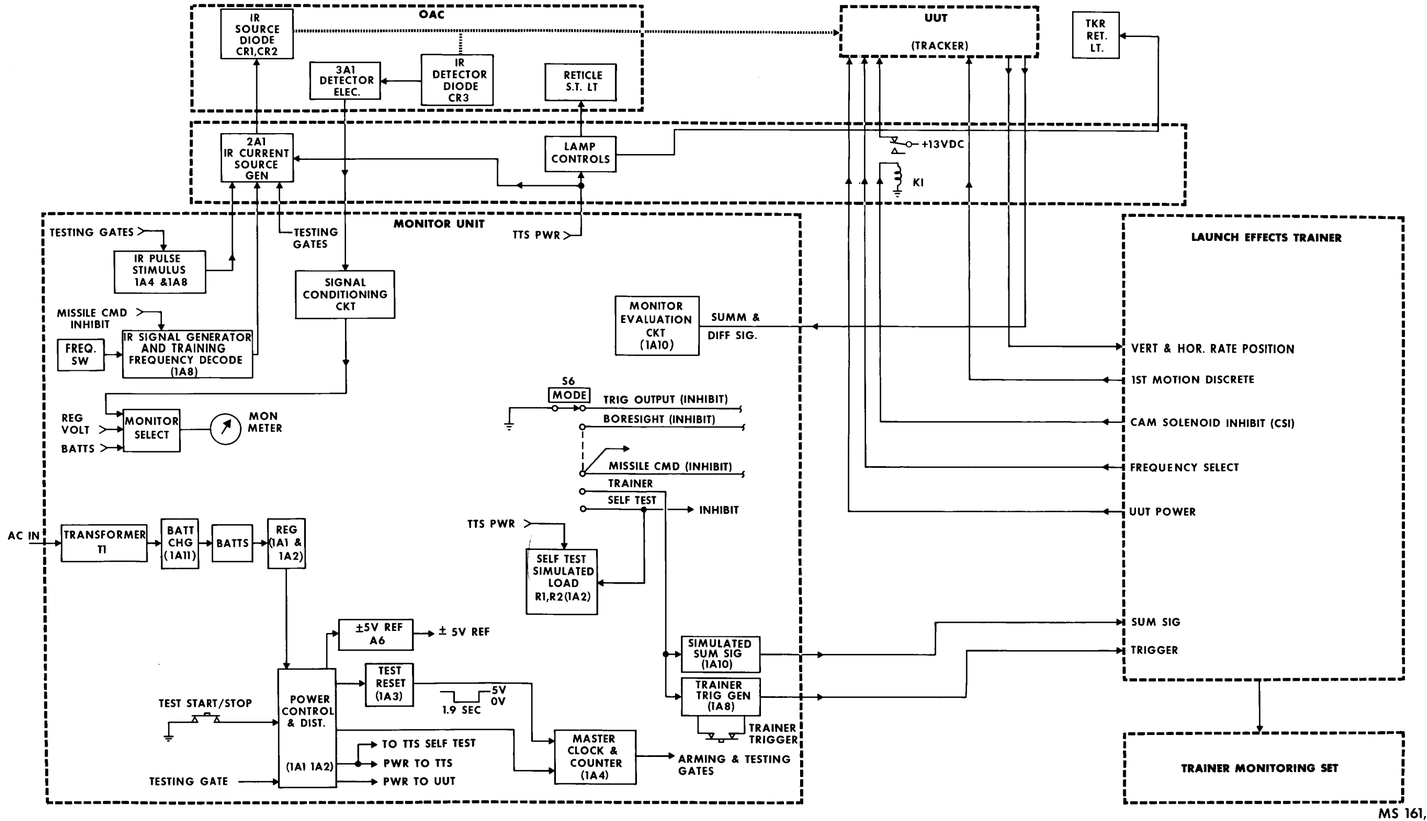

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Figure 2-2 Tracker test set with trainer monitor block diagram

(b) The TTS provides a simulated sum signal from card 1A10 to the MTS.

(c) The TTS provides a simulated trigger firing pulse from TTS card 1A8 initiating the operation of the UUT, LET and MTS. In the trainer mode, the MTS provides the power for the operation of the UUT. The testing indicator will illuminate upon depression of the test start/stop switch and the OAC diode CR1 will emit IR energy modulated at the training frequency. Upon depression of the trainer trigger switch, the simulated sum signal is applied to the MTS. With known vertical and horizontal alignments of the IR source with respect to the UUT, the MTS will respond with a predicted score. The go and no-go indicators are not enabled in the trainer mode of operation. The trainer mode of operation is not a timed function of the TTS. Termination of testing is accomplished by depression of the test start/stop switch.

2-2. Subassembly Operational Description.

The monitor unit contains the battery packs, battery charger, power regulators, stimuli generators, evaluation circuitry, and the controls, indicators, and interconnect points necessary for test operation.

a. Monitor Unit Panel Controls, Indicators and Interconnect Points.

(1) INTERCONNECT 1J1 is used to interconnect the monitor unit to the OAF.

(2) TEST 1J2 is used to connect the monitor unit to test equipment used during checkout of the TTS.

(3) TRAINER TRIGGER switch is a momentary switch which, when depressed in the trainer mode, applies a simulated UUT firing pulse to the LET and produces a simulated sum signal to the UUT.

(4) MONITOR meter provides the operator with a visual indication of the charge condition of the battery packs, the voltage regulator outputs, and the IR diode output level.

(5) MONITOR SELECT switch is used during self-test to select the parameter to be displayed by the monitor meter.

(6) The three FUNCTION indicators present the TTS and UUT status during a test cycle. The TESTING indicator will illuminate upon depression of the test start/stop switch and will extinguish in the trig output, boresight, and missile command modes at Ts +21 seconds. At Ts +21 seconds, the monitor unit will make a logic decision and the appropriate indicator will illuminate. If the test results in a go decision, the GO indicator will be illuminated in the boresight and missile

command modes until Ts +30 seconds. If the test has failed, the NO-GO indicator will be illuminated in the boresight and missile command modes until Ts +60 seconds.

(7) TEST START/STOP switch is a momentary switch which initiates the test start function. This switch energizes or deenergizes the power-on relays, applying or removing power from the test set circuits. At Ts +6 seconds the operator may re-actuate the test START/STOP switch and stop the test sequence.

(8) MODE switch provides the means to select any of the five major modes of operation: SELF TEST, TRIG OUTPUT, BORESIGHT, MISSILE CMD, and TRAINER. The switch also provides the means to identify the fault after a no-go condition in the bore-sight and missile command modes.

(9) FREQUENCY switches are enabled in the missile command mode and are used by the operator to select any one of 100 discrete frequencies for the IR source stimuli. One switch is the 10 switch and the other is the units switch.

(10) BATTERY indicators provide a visual indication of the charge condition of the battery packs during battery charging. The FULL CHARGE indicator will illu-minate when the battery packs reach 80 percent of full charge and the battery charger switches to the low charge rate of 300 ma per hour. The CHARGING indicator is illuminated when the battery charger is operating at the high charging rate of 600 ma per hour. The CHARGING indicator will illuminate during the performance of any major test.

(11) EXTERNAL POWER 1J3 interconnects the battery charger with a power source. The power required for the battery charger is 105-130 Vac, single phase, 50-440 Hz.

(12) CHARGE switch is a 1-amp circuit breaker used to apply external power to the battery charger.

(13) POWER switch is a 2-amp circuit breaker which applies battery pack power to the power-on relay.

b. Monitor Unit Battery Charger (fig. 2-3). The ac input to the battery charger is coupled through the RFI filter and CB2 to the primary of isolation/step-down transformer T1. The 65 Vac output of T1 is coupled to a bridge rectifier/ filter on 1A11.

(1) Positive dc from the bridge rectifier/filter is fed to the charge current control amplifier, the power regulator, and the load sharing shunt resistor. This voltage source actuates relay K2.

(2) In the high-charge state relay K1 is deenergized. In this position, load sharing shunt resistors R3 and R4 are in parallel and R5 and R7 are in parallel, decreasing total resistance. This low resistance increases charge current to the

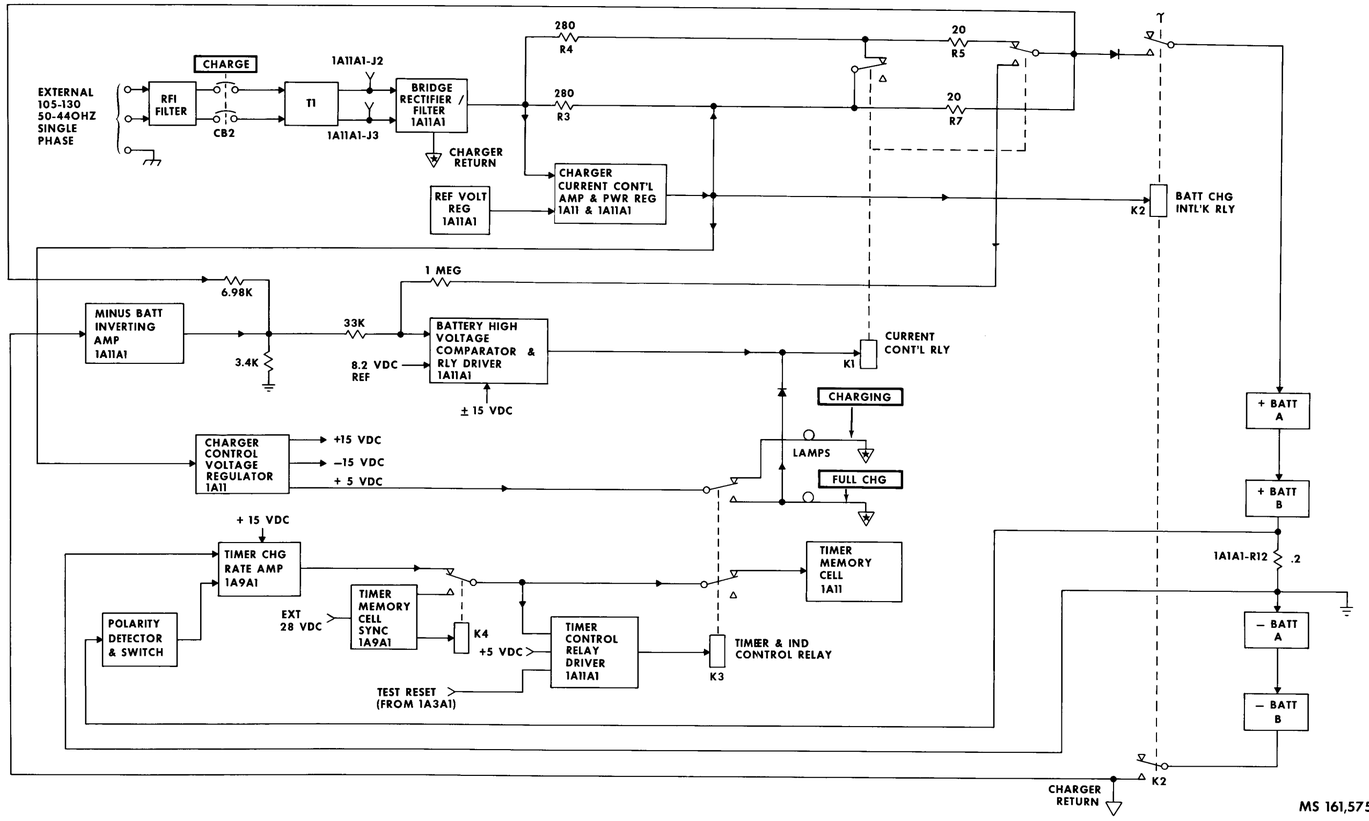

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Figure 2-3 Battery charger - functional block diagram.

high rate of 600 ma. The charger current control amplifier and power regulator maintains a constant current through R5, R7, and the batteries. Current is passed through the batteries in series, returning to the minus terminal of the bridge/ rectifier/filter through the energized contacts of K2. The charger control voltage regulator provides regulated ±15 Vdc operating voltages. The ±15 Vdc auxiliary regulator applies power to the battery high voltage comparator, timer current control relay driver, and timer charge rate amplifier.

(3) The 8.2 Vdc high voltage reference is regulated down from the +15 Vdc auxiliary power for operation of the battery high voltage comparator. The minus battery inverting amplifier provides a scaled output voltage which is summed with an attenuated plus battery charge voltage and then fed to the battery high voltage comparator. This voltage is scaled to a factor of 0.32 volts for each volt from the battery pack. When the battery charger voltage rises to 80 percent capacity (32.0 volts), the battery high voltage comparator will actuate the current control relay driver, energizing K1. When K1 energizes, R4 and R5 are removed from the circuit causing a total impedance rise and a resultant current decrease through the batteries. This charge rate is 300 ma. Deplating time is dependent upon current input. Replating is achieved by polarity reversal. Deplating of the cell begins when current is passed through it. When the cell is plated, it acts as a low resistance to ground and after the timer memory cell has fully deplated, the resistance changes from a low value to a very high value. This drives the timer control relay driver and energizes K3. When K3 energizes, the battery charging indicator switches from charging to full charge. The timer synchronizing circuit allows for external synchronization of the timer memory cell with an external +28 to +30 Vdc.

c. Monitor Unit Battery Packs (fig. 2-3). The monitor unit has four battery packs, one mounted in each corner of the chassis, which provide primary power for the TTS and UUT. The battery packs are designated +batt A, +batt B, -batt A, and -batt B. Each battery consists of eight series-connected “D” cells. Each pack has a 10.0 Vdc, 3.5 amp-hour nominal rating. The outputs are fed via CB1 to the contacts of the primary power interlock relay.

d. Power Supplies, Mode Relays and Diode Matrix Circuit (fig. 2-4 and 2-5). There are five primary regulated power supplies in the monitor unit. The power supplies are: + and -13 Vdc, + and -5 Vdc reference, and +5 Vdc digital. The + and -13 Vdc provide UUT power and are used for general test set operation. The + and -5 Vdc reference are reference voltages provided for TTS circuitry. +5 Vdc

digital is utilized by the logic units of the evaluation circuits. Power is distributed through functional relays, which are controlled by the monitor unit mode switch. Overvoltage protection for the +13, -13 and the +5 Vdc digital supplies is provided by crowbar circuits, which will reenergize the primary power interlock relay whenever an overvoltage condition is sensed.

(1) The + and -13 Vdc supplies and +5 Vdc digital supply (fig. 2-4) input is from the plus and minus battery banks. Voltage supplied through CB1 to the X coil of K1 causes it to energize when the test start pushbutton is depressed, if the mode switch is in the correct position. The battery voltage is then coupled through filters to the DC-AC inverter, the +13 Vdc series regulator, and the -13 Vdc series regulator. The output of the +13 Vdc regulator is coupled to the +13 Vdc overvoltage crowbar, which provides overvoltage protection. The output of the -13 Vdc regulator is coupled to the -13 Vdc overvoltage crowbar, which drives electronic switch Q1, providing overvoltage protection. The AC output from the DC-AC inverter is coupled to a full-wave rectifier/filter. The rectified DC output is coupled to the +5 Vdc switching regulator, where it is regulated to +5 Vdc. The output of card 1A1 pin 9 is fed to the +5 Vdc overvoltage crowbar and the distribution on card 1A2.

(2) The + and -5 Vdc reference supply and the mode select and diode matrix for power distribution are depicted in figure 2-5.

e. Tracker Optics Stimulation (figs. 2-6 and 2-7). For checkout of the UUT systems, the OAC IR collimated source is programmed in IR position, modulation frequency, and IR intensity. This input simulates the missile position during flight. Each stimuli parameter is discussed below.

(1) In the boresight mode the IR position simulates a missile on the line sight (foresight). The OAC radiating diode (IR source) used in foresight mode located in the OAC and is referred to as the near-center diode. The alignment between the TTS OAC and the UUT is performed manually by adjustments on the OAC, and by use of an optical assembly. The optical assembly enables alignment of the UUT sight with respect to an optical reference. The optical reference is aligned with respect to the IR source. In the missile command mode the IR position simulates a missile that is off the line of sight to the right and down. The radiating diode (IR source) is located in the OAC and is referred to as the near-center diode. The alignment between the TTS OAC and the UUT is performed manually by adjustments on the OAC. In the boresight mode a dynamic gain test (off boresight shift) is

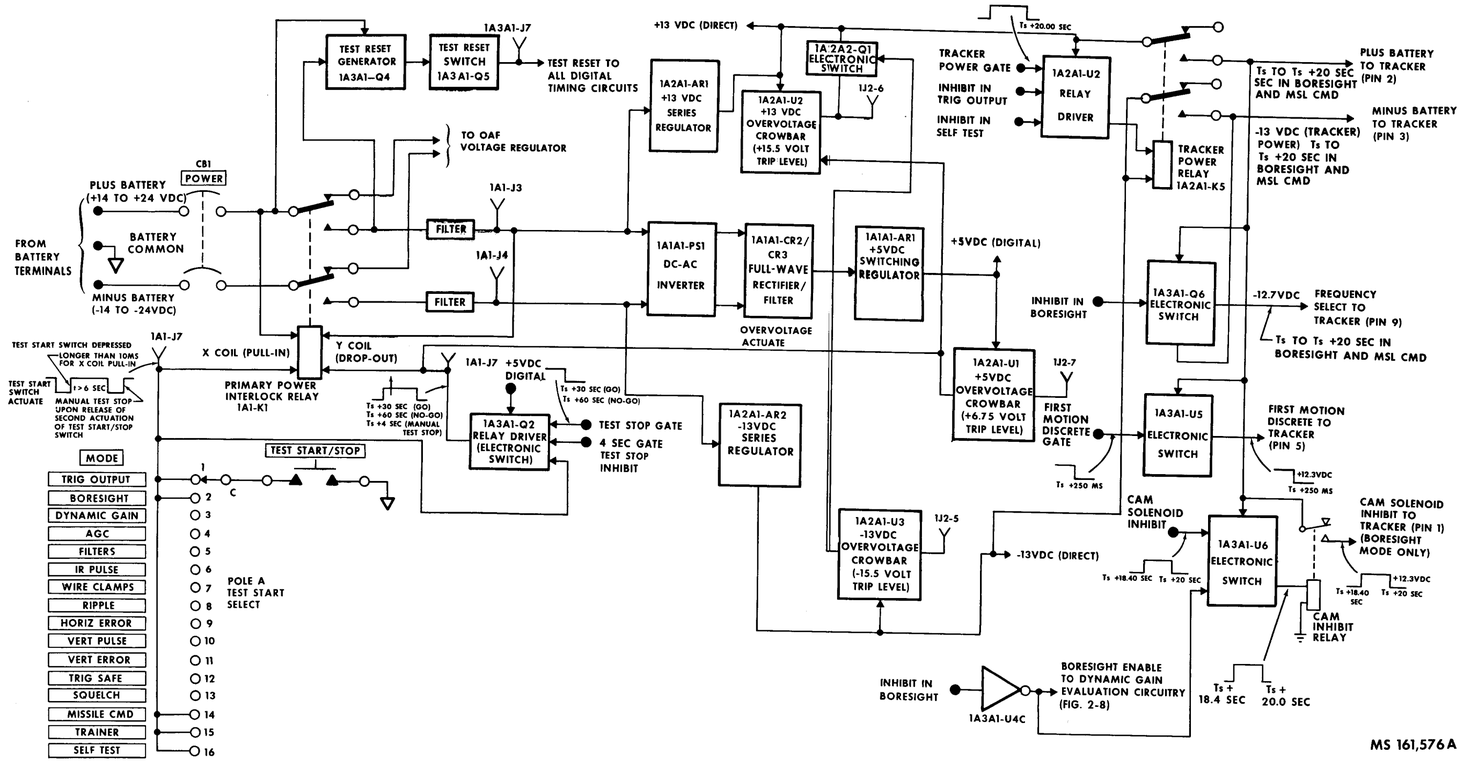

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Figure 2-4. Plus and minus 13VDC, and plus 5 VDC digital regulator power supplies - functional block diagram

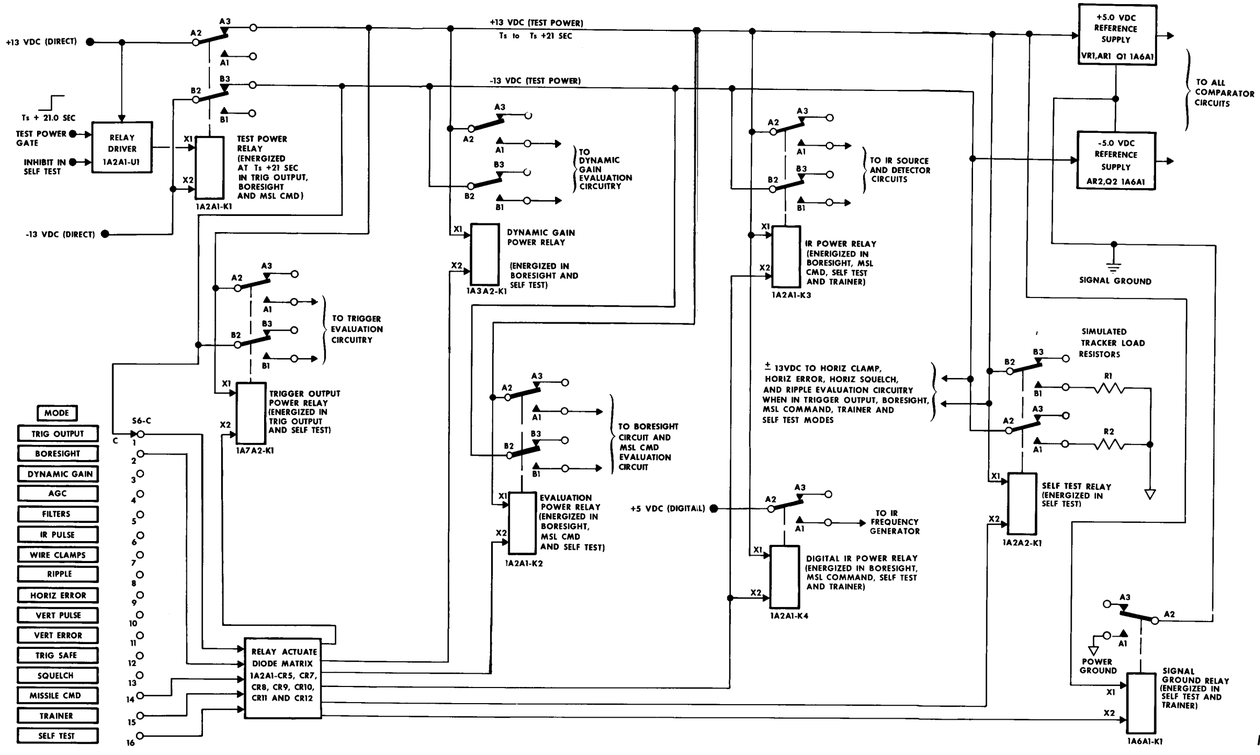
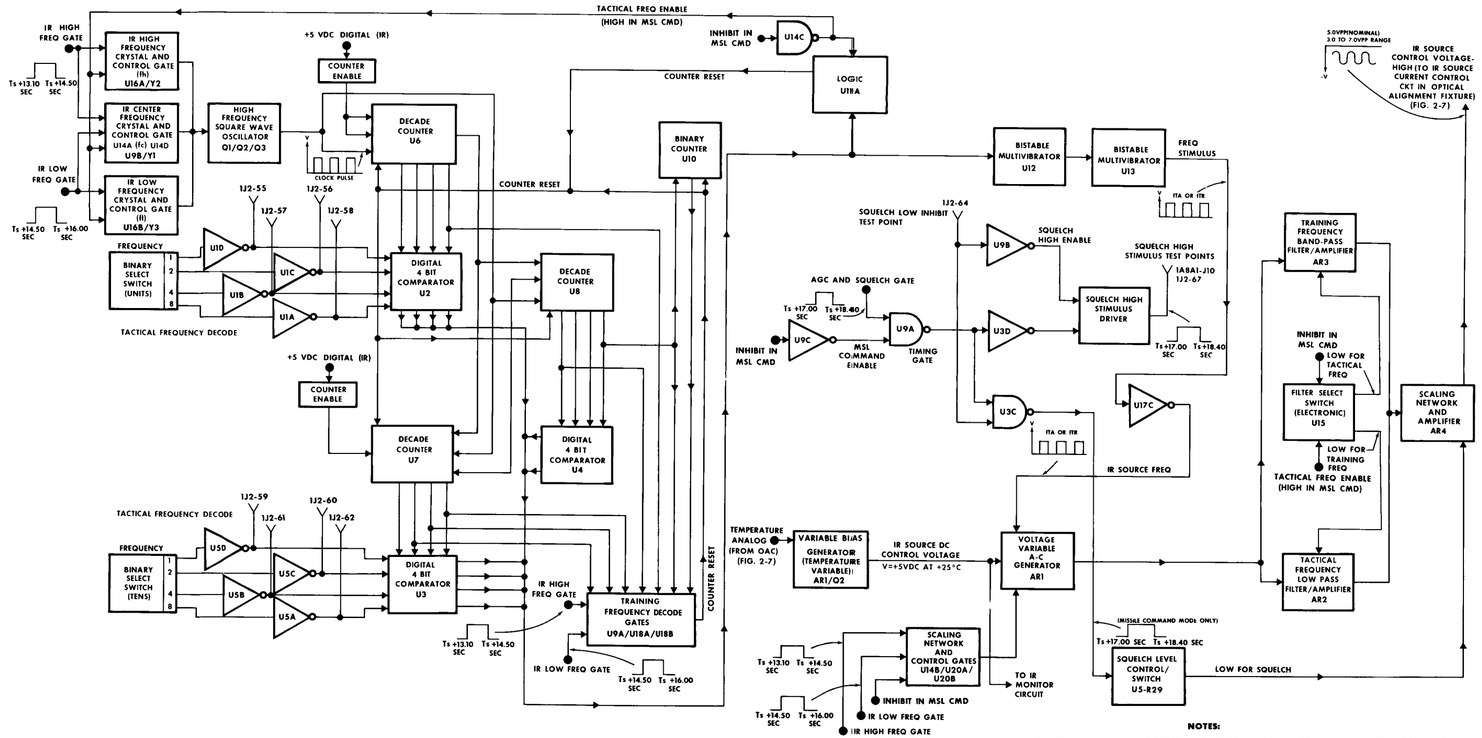


Figure 2-5. Plus and minus 5.0 volt reference supply, mode select and relay matrix - functional block diagram



NOTES:

1. + AND -13 VDC APPLIED TO 1A8A1-AR1 THRU AR3 AND 1A8A2-AR1 AND AR4 ONLY IN BORESIGHT, MSL CMD, SELF TEST AND TRAINER MODES.
2. ALL CIRCUITRY SHOWN IS LOCATED ON CARD 1A8A2 UNLESS OTHERWISE INDICATED.

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Figure 2-6. Infrared stimulus control - functional block diagram.

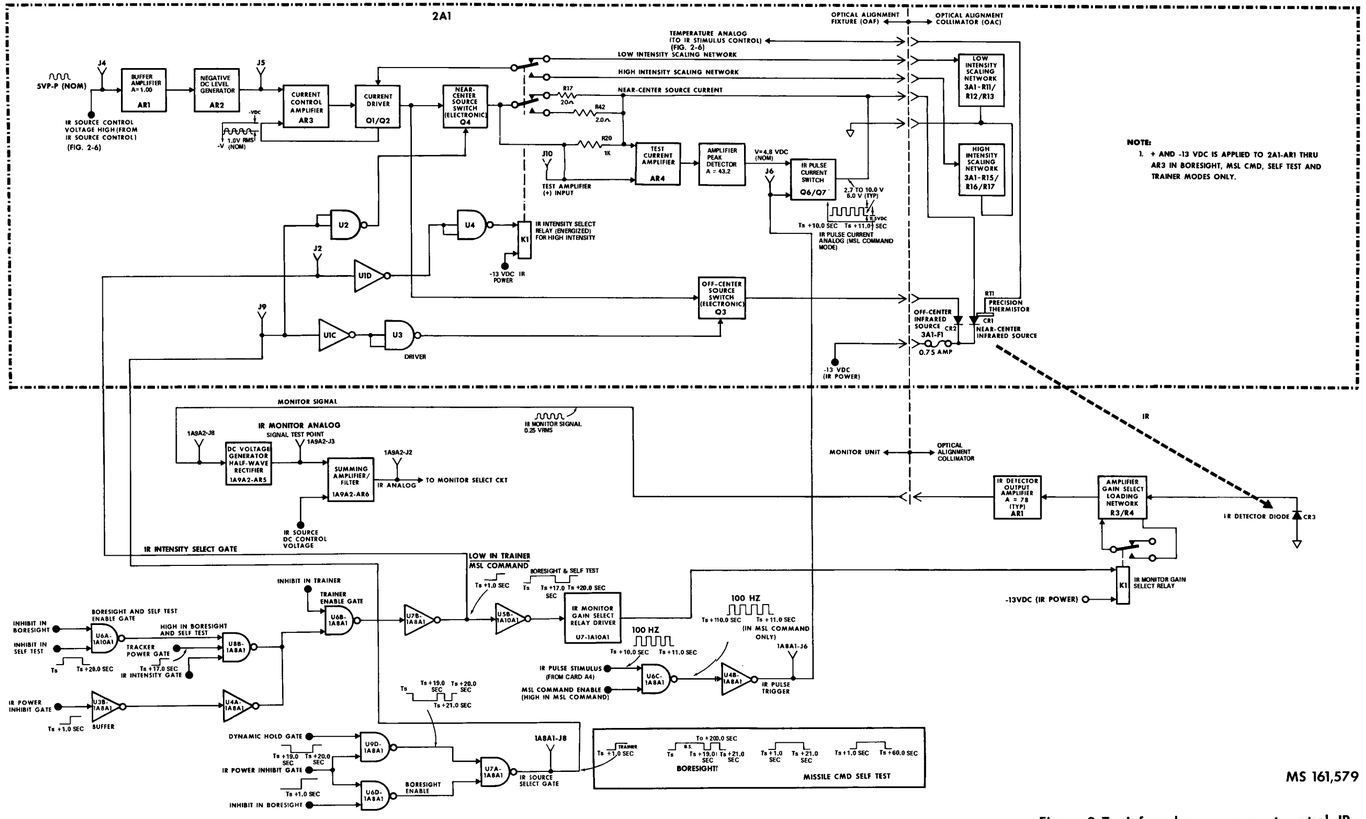

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Figure 2-7. Infrared source current control, IR monitor and IR source control logic - functional block diagram

performed. This configuration is used to simulate a missile movement from a boresight line of sight to an off boresight line of sight. A second IR source, called the off-center diode, is activated during the test sequence which shifts the IR output from a on-center position to an off-center position. This shift gives the UUT a rate-change.

(2) The IR intensity is controlled by the 2A1 card in the OAF. The different levels of intensity emitted for each test mode are as follows:

(a) In the boresight and missile command low intensity modes, with the near center diode activated, the nominal TTS radiation AC intensity is 1.84×10^{-10} watts/cm^2. This configuration nominally stimulates the UUT to give a nominal value to the dynamic gain, AGC, filter, vertical error, and horizontal error circuits.

(b) In the foresight and missile command high intensity modes, the TTS OAC near-center diode current is increased approximately 65 times nominal. In the foresight mode the high intensity is activated at Ts through Ts +1 second and at Ts +17 through Ts +20 seconds to put the UUT into AGC. In the missile command mode, the high intensity is activated only at Ts through Ts +1 second.

(c) The dynamic gain high intensity test is performed in the boresight mode. In this test the TTS IR intensity is switched from the on-center high intensity level to the off-center high intensity level at Ts +19 seconds. This OAC IR position shift gives a rate/position change input to the UUT.

(d) The squelch low intensity test is performed in the missile command mode. At Ts +17 seconds, the OAC near-center diode IR intensity is reduced to 85 percent of the nominal level. This attenuation evaluates the UUT while it is in squelch mode.

(3) The IR signal to the UUT is modulated at either of two major frequencies, training or tactical. The IR frequencies for each test mode are as follows:

(a) For all TTS boresight and training mode tests, the center training frequency is used. The training frequency is 5 kHz ± .5 percent.

(b) For all TTS missile command mode tests, the center tactical frequency is used. The frequency is selected by positioning the 100 position digit switch (on the TTS monitor unit) to the proper code number.

(c) In the boresight and missile command modes, the Infrequency (modulation) is shifted to a plus percent of the IR center frequency at Ts +13.1 seconds in the test sequence. At Ts +14.5 seconds the modulation frequency is shifted to a minus percent of the center frequency. This IR frequency shift evaluates the UUT filter circuits in the tracker. The TTS verifies that when the UUT is operated at the

training or tactical frequency the voltage amplitude (on the UUT sum and difference parameters) at the upper and lower cutoff frequencies (as described above) shall be 2 db down from the value at the respective center frequencies.

(d) The IR pulse stimuli is a false sample test which is performed in the TTS missile command mode at Ts +10 seconds through Ts +11 seconds. The TTS OAC generates a series of IR pulses during the 1 second interval. The pulse repetition rate is 100 PPS, the IR intensity is as earlier described, and the pulse width is 20 microseconds (measured at the 30 percent amplitude points). This signal is at the nominal tactical modulation frequency. The objective of this test is to evaluate the UUT's ability to reject the processing of a false sample pulse.

(4) Two IR emitting diodes and one IR detector diode are located in the OAC. The emitting diodes transmit IR energy to the UUT. The emitting diodes current flow determines the IR intensity. This current is modulated to the UUT training or tactical frequency (fig. 2-7). The current flow for the near-center IR diode at low intensity is from card 2A1 ground through scaling resistors R11/R12/R13 and R15 in 3A1 to card 2A1, through K1 (normally closed contacts), through current drivers Q1/Q2, through near center source switch Q4, through K1 to sealing resistor R17/R20 to near-center diode CR1. The cathodes of CR1 and CR2 are tied to -13 Vdc. This direct current flow is modulated by current drivers Q1/Q2 which are controlled by amplifiers AR1/AR2/AR3. The input to AR1 on card 2A1 is the IR source control voltage which is a nominally 5 VP-P sine wave signal generated on card 1A8 (this circuit will be discussed later).

(a) From Ts to Ts +1 second in missile command mode or boresight mode (and from Ts +17 seconds to Ts +20 seconds in the boresight mode), relay K1 actuates, which changes the scaling resistors from 20 ohms (R17) to 2 ohms (R42), and switches to R15/R16/R17 on card 3A1. This lower resistance path increases the current flow through CR1 diode providing a high intensity IR current.

(b) In the missile command mode between Ts +10 seconds and Ts +11 seconds, a 100 Hz square wave pulse, generated in card 1A4 and buffered in card 1A8A1, is superimposed on the modulated direct current through the CR1 IR diode. This is performed by AR4, AR5, Q5, Q6, and Q7.

(c) In the TTS boresight mode at Ts +19 seconds, the near-center IR diode CR1 is turned off and the off-center IR diode CR2 is turned on. [The intensity remains high (K1 energized) in this mode]. This occurs when U7A on TTS card 1A8A1 turns Q4 off and Q3 on through U2, U1C, and U3. The current path is now from

ground through scaling resistors R15/R16/R17, through K1 (energized), through current drivers Q1/Q2, through switch Q3 to off-center diode CR2.

(d) IR detector diode CR3 is used to detect the radiated output from the IR source diodes. The output from CR3 is connected to a resistive network controlling the gain of amplifier 3A1-AR1. This gain is controlled by the operation of 3A1-K1 and is used to maintain a constant output to the monitor meter when the emitting diode is switched from low intensity to high intensity.

(5) The IR source control voltage is generated on card 1A8. The block diagram is shown in figure 2-6. The IR source control voltage is a sine wave with the following programed characteristics:

(a) The two basic frequencies for IR source control signal are the 5 kHz training frequency (used in the TTS boresight mode and the trainer mode) and the tactical frequency (used in the TTS missile command mode). These two basic frequencies are outputs of the counters U6/U7/U8/U10, comparators U2/U3/U4, decode gates U9A/U18A/U18B, multivibrators U12/U13, and logic U11A/U14C. In the missile command mode the counters are controlled by two binary select switches. The high frequency oscillator Q1/Q2/Q3 is controlled by one of three crystals Y1/Y2/Y3. At Ts +13.1 seconds to Ts +14.5 seconds, U16A logic enables the Y2 crystal which controls the high frequency oscillator. This crystal provides a frequency 3.5 percent higher than the center tactical frequency. From Ts +14.5 seconds to Ts +16.0 seconds, U16B logic enables the Y3 crystal, which provides an output frequency which is 3.5 percent lower than the tactical frequency. The high and low tactical frequencies are used in conjunction with the center tactical frequency to evaluate the UUT tuned filters as previously described. At all other times while in the missile command mode, U9B logic enables the Y1 crystal which provides the center tactical frequency. The square wave pulse train output from U12/U13 is inverted by U17C, converted to a sine wave by AR1, and filtered and amplified by AR2. The sine wave is further amplified by scaling amplifier AR4 and then fed to card 2A1. In the missile command mode, a squelch test is performed from Ts +17.0 to Ts +18.4 seconds. At this time the squelch level control switch U5 reduces the scaling, thus reducing the output frequency voltage level from AR4 to 85 percent of its normal level. This causes the UUT to go into a squelch condition for a squelch test as previously described.

(b) In the boresight mode U9B enables the Y1 crystal only. The counters are controlled by the training frequency decode gates U9A/U18A/U18B, and provide a sine

wave output from AR1 at 5 kHz. In this mode the filter select switch U15 operates to select the output from AR3 which provides filtering for the training frequency. After amplification the 5 kHz signal is routed to the scaling amplifier AR4 and then to card 2A1. The output from AR4 is approximately 5 VP-P. In this mode from Ts +13.1 to Ts +14.5 seconds the training frequency decode gates U9/U18A/U18B select the higher training frequency. In boresight mode this frequency change is produced by a signal change to the counters instead of changing crystals. The logic will also select a low training frequency from Ts +14.5 to Ts +16.0 seconds. The frequency shift is ±7.O percent of center frequency for checking the UUT tuned filters while using the training frequency.

f. Evaluation Circuitry (figs. 2-8 through 2-18). The monitor unit contains the circuitry which evaluates the UUT outputs. The major operational modes were discussed in paragraph 2-1. The individual tests performed in the boresight, trigger output and missile command modes are discussed in the following paragraphs. Time reference in this description is TTS time. UUT Ts occurs 250 msec after test set Ts. Only that data of a general nature or pertinent facts which are not obvious on the associated block diagrams are discussed.

(1) The dynamic gain test is performed during the boresight mode. The IR stimuli for the UUT is switched from the near-center diode to the off-center diode and the IR intensity is increased. This switching provides a rate position change in the UUT. The TTS monitor measures the UUT horizontal and vertical rate position shift and verifies it to be $\geq$ 6.1 Vdc for horizontal and $\geq$ 4.5 Vdc for vertical for 200 msec after the IR position change. The rate position outputs are routed via OAF connector 2J3 pins 10 and 11 to the inverting amplifier's AR1 (vertical) and A24 (horizontal) on TTS card 1A9 (see fig. 2-10). These amplifiers invert the signal which is then fed to card 1A3 (see fig. 2-8). Before the IR position shift, the signal level is passed by switch U8 and stored by the sample and hold circuits AR1 and AR3, which establishes a nominal reference level to differential amplifiers AR2 and AR4. At Ts +19 seconds, U8 is switched off and the OAC IR source is switched. This IR position shift causes the UUT rate outputs to shift. This signal is fed directly to differential amplifiers AR2 and AR4 and compared with the reference voltage from the sample and hold circuit. If the voltage differentials are $\geq$ 6.1 Vdc for horizontal and $\geq$ 4.5 Vdc for vertical, the outputs of U7 and U9 will switch high. The logic verifies that this voltage change occurs within 200 msec. after the IR positions shift and has decayed to < 6.1 Vdc for horizontal and < 4.5 Vdc for vertical within 500 to 600 msec.

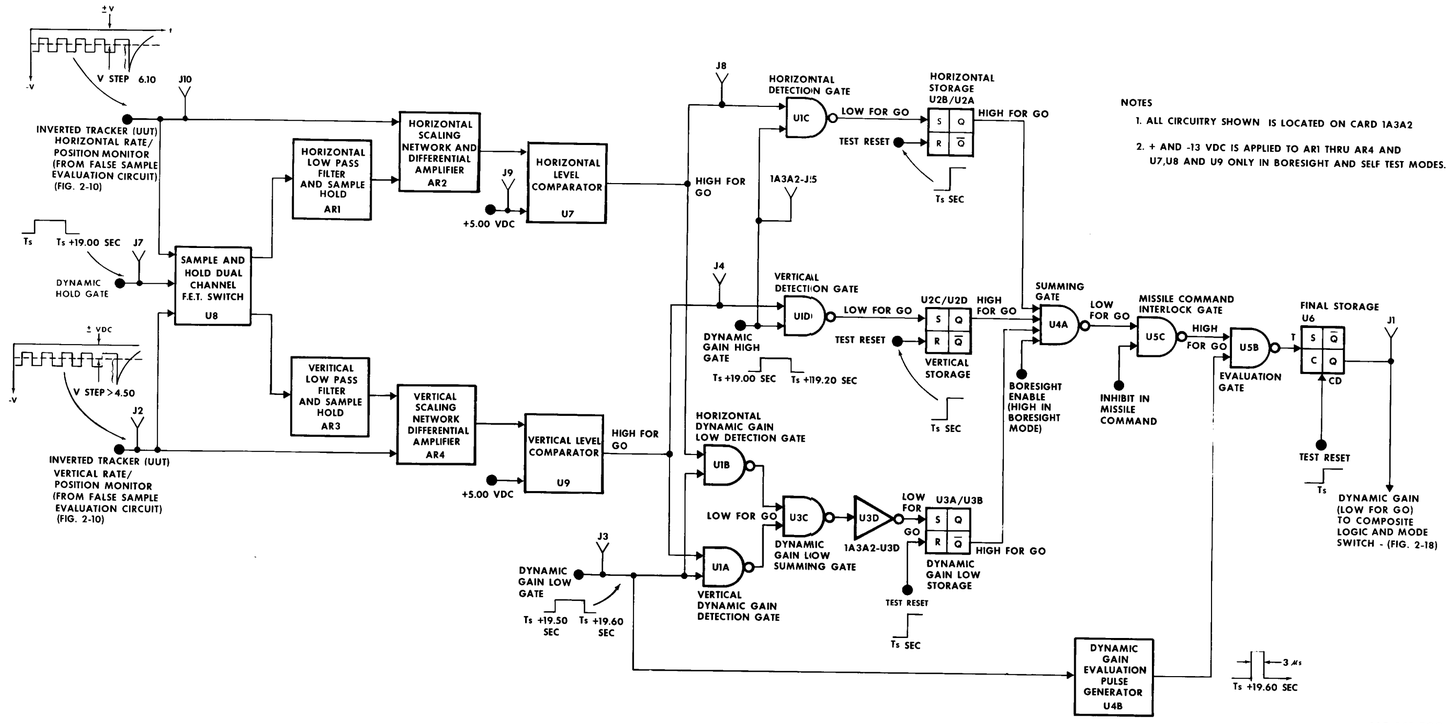

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Figure 2-8. Dynamic gain evaluation - functional block diagram

(2) Much of the circuitry of card 1A10 is used for both automatic gain control and filters test evaluation. The automatic gain control (AGC, fig. 2-9) test verifies that the UUT sum and difference signal levels are a minimum of 8.2 VP-P and maximum of 20 VP-P during a period when the IR intensity is increased a minimum of 70 times above the nominal intensity level. This test is conducted in boresight mode only, from Ts +17.0 to Ts +18.4 seconds. The UUT signal is routed through connector 2J3 pin 12 (difference signal) and pin 13 (sum signal), conditioned by voltage divider circuits which are controlled by U1. The mode gain select switch U1 has two fixed gain outputs. In the AGC mode, the low output from U13 causes the gain to be 0.1058. The scaled outputs are fed to peak detectors AR1 and AR3 and then evaluated by high-low comparator circuits U2, U3, U5 and U7. The comparator outputs are summed by U8B and fed to U9B. U9B is enabled by the U8A circuits. The pulse delay generator U8A delays only the leading edge of the AGC squelch gate by 420 msec and has an inverted (negative gate) output. This delay in enabling the AGC logic gives the UUT time to stabilize after the OAC IR intensity changes at Ts +17.00 seconds.

(3) In the filters test (fig. 2-9), the OAC IR source modulated frequency is increased to the UUT upper band pass limit. This occurs at Ts +13.1 through Ts +14.5 seconds. At Ts +14.5 seconds, the frequency is shifted to the lower band-pass limit. This frequency shift is used for evaluation of UUT sum and difference filters. The monitor unit verifies the voltage amplitude limits of the UUT sum and difference signals shifts with respect to the frequency. The UUT sum and difference signal is fed to TTS card 1A10A2 and is conditioned by a divider/detector circuit prior to being fed to peak detectors AR1 and AR3. The filters test is initiated at Ts +13.0 seconds and is terminated at Ts +16.0 seconds. Much of the same circuitry used for AGC test [para. 2-2 f (2)] is also used for the filter test.

(a) For the filter test, the mode channel gain select switch U1 is now changed to a gain of 1.00 by the high output from U13 on 1A10A1 at Ts +16.0 seconds. From Ts to Ts +13.1 seconds the UUT is modulated at the center frequency. The resultant sum and difference signal levels at the output of AR1 and AR3 and the RC filters are fed to both the U4 and U6 comparators and through the normally closed contacts of K1 to the sample and hold circuits AR2 and AR4. The sampled value is supplied to comparators U4 and U6 as a reference level. At Ts +13.0 seconds, relay K1 is energized, opening the signal path to the sample and hold circuits AR2 and AR4. At Ts +13.1 seconds, the IR source frequency modulation is shifted to the

upper band-pass of the UUT filters. The outputs from the UUT are now routed to comparators U4 and U6 where they are compared with the center frequency levels stored by sample and hold circuits AR2 and AR4. At Ts +14.5 seconds, the IR source frequency is shifted to the lower band-pass of the UUT filters, and the same comparison occurs. The sum and difference voltage amplitude at the upper and lower cut-off frequencies shall be 2.00 db down from the value at the respective center frequencies. If the outputs of the UUT filters (sum and difference channels) are within these specifications, the outputs of U4 and U6 will each be high for a go condition.

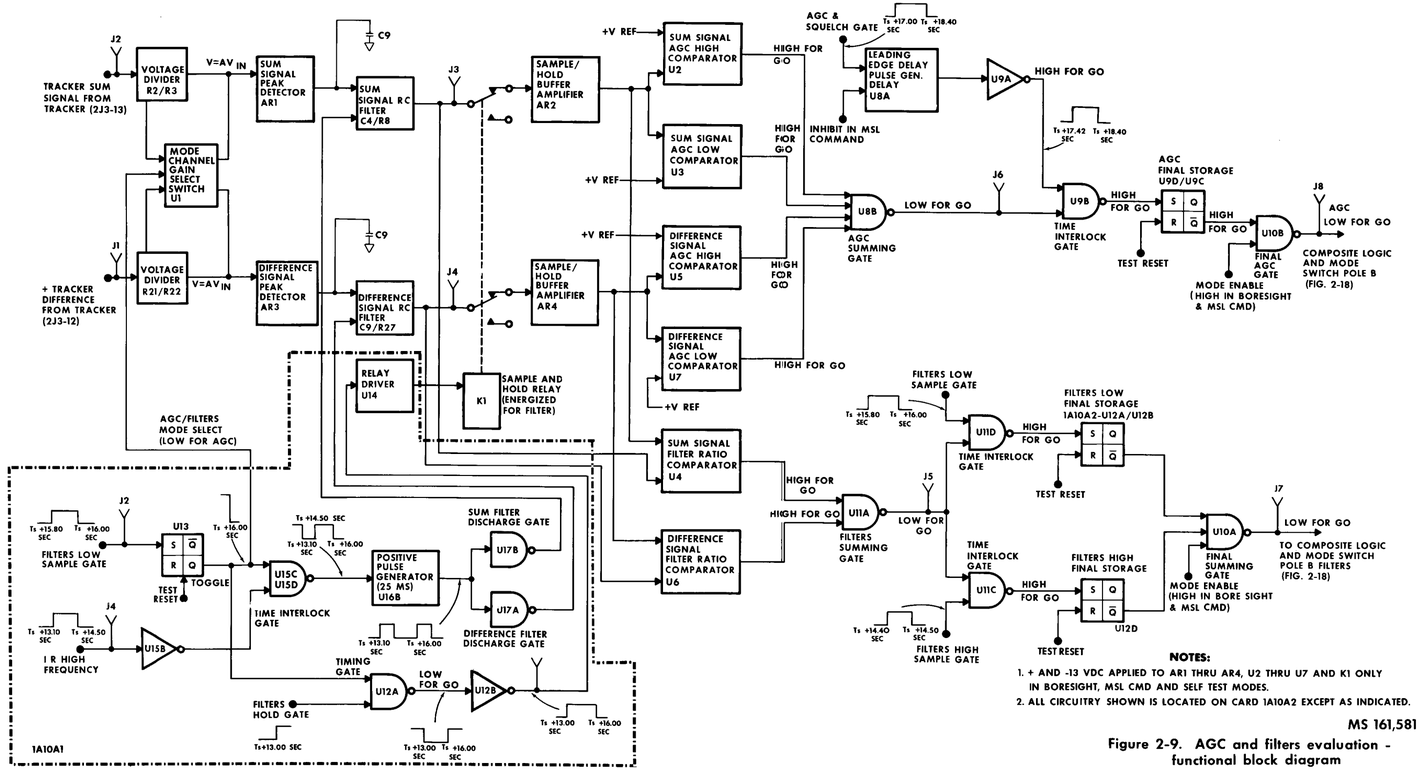
(b) U16B provides a positive 25msec wide pulse at Ts +13.1 and Ts +16.0. seconds to U17A and U17B on 1A10A1 to allow discharge of the peak detector holding capacitors C4 and C9 on 1A10A2 after the IR source frequency shift.

(4) An IR pulse test of 1 second duration is initiated at Ts +10.0 seconds in the missile command mode of operation. The object of this test is to stimulate the UUT in a manner to produce a false sample in the horizontal and vertical rate circuits. The TTS generates a 100 Hz IR pulse superimposed on the nominal sinosodial IR output. The UUT vertical and horizontal rate position output signal is evaluated to determine if the UUT has detected and responded properly to the simulated IR noise pulse. Cards 1A9 and 1A10 are used for the evaluation of the squelch, and IR pulse test.

(a) The vertical and horizontal rate position signals from the UUT (fig. 2-10) are inverted and scaled by AR1 and AR4, derated, filtered, and then amplified by AR2 and AR3. If any UUT pulse after being derated exceeds the average de-rated level by more than ±1.0 Vdc, the appropriate false sample comparator U2, U5, U1 or U4 will switch low causing summing gate U3 output to go high and U9A output to go high for a no-go.

(b) The derate networks remove the rate and the dc offset voltage and retains the signal data. The signal will now swing positive and negative through a zero reference. AR3 and AR2 are linear amplifiers with a gain of 5.23.

(5) Wire clamp. This test is performed in both the boresight and missile command modes. Evaluation circuitry is located on cards 1A5 and 1A6, as shown in figure 2-11. The TTS verifies that no signal greater than 0.500 volt peak is generated on the UUT horizontal guidance wire in the time period Ts through Ts +350 msec (100 msec after UUT first motion discrete signal). The monitor unit also determines that no signal greater than 0.500 volt peak is generated on the UUT vertical guidance wire until after Ts +701 msec (451 msec after UUT first motion).



NOTES:

1. + AND -13 VDC APPLIED TO AR1 THRU AR4, U2 THRU U7 AND K1 ONLY IN BORESIGHT, MSL CMD AND SELF TEST MODES.
2. ALL CIRCUITRY SHOWN IS LOCATED ON CARD 1A10A2 EXCEPT AS INDICATED.

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Figure 2-9. AGC and filters evaluation - functional block diagram

NOTES

1. ALL CIRCUITRY SHOWN IS LOCATED ON CARD 1A9A2 EXCEPT AS INDICATED.
2. + AND -13 VDC APPLIED TO AR1 THRU AR4 AND U1, U2, U4, AND U5 ONLY IN BORESIGHT, MSL CMD AND SELF TEST MODES.

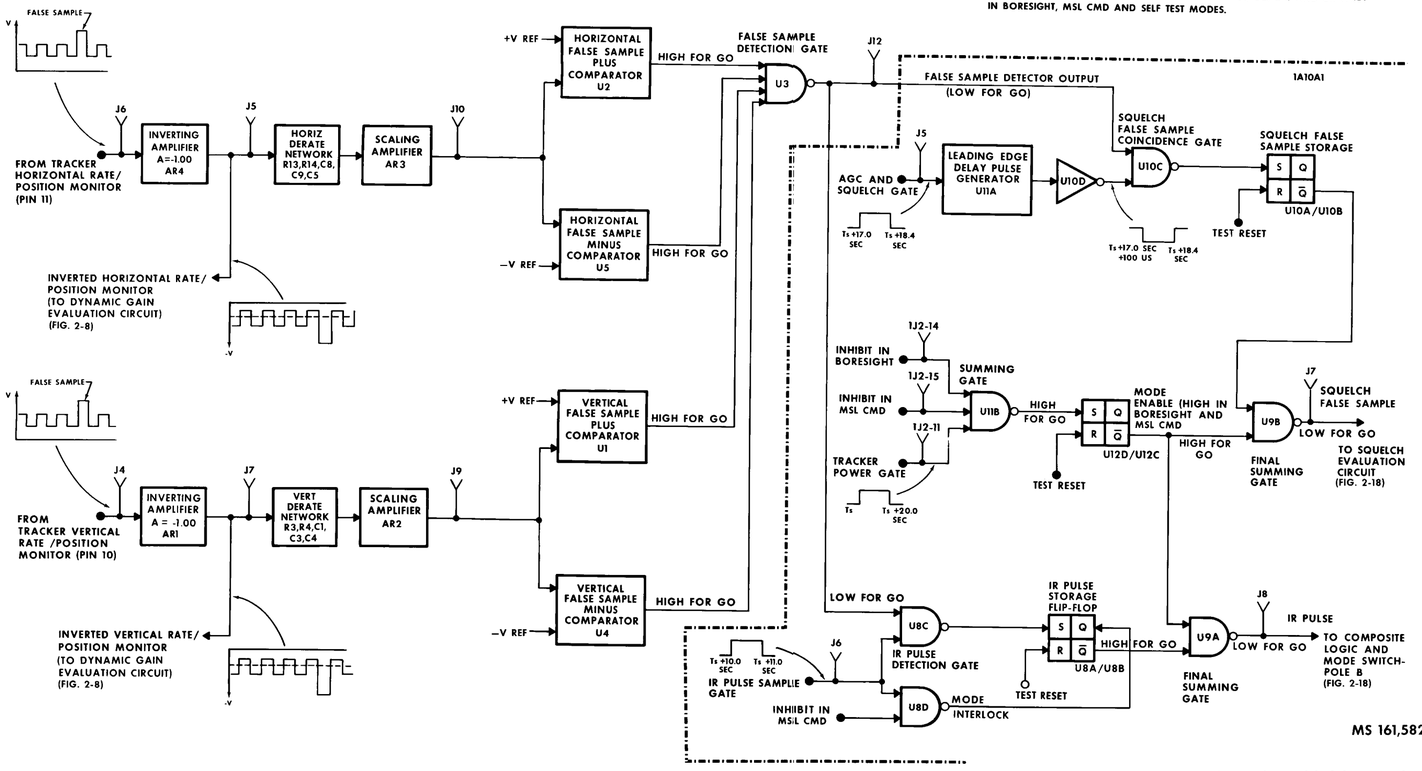

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Figure 2-10. IR pulse and squelch false sample - functional block diagram.

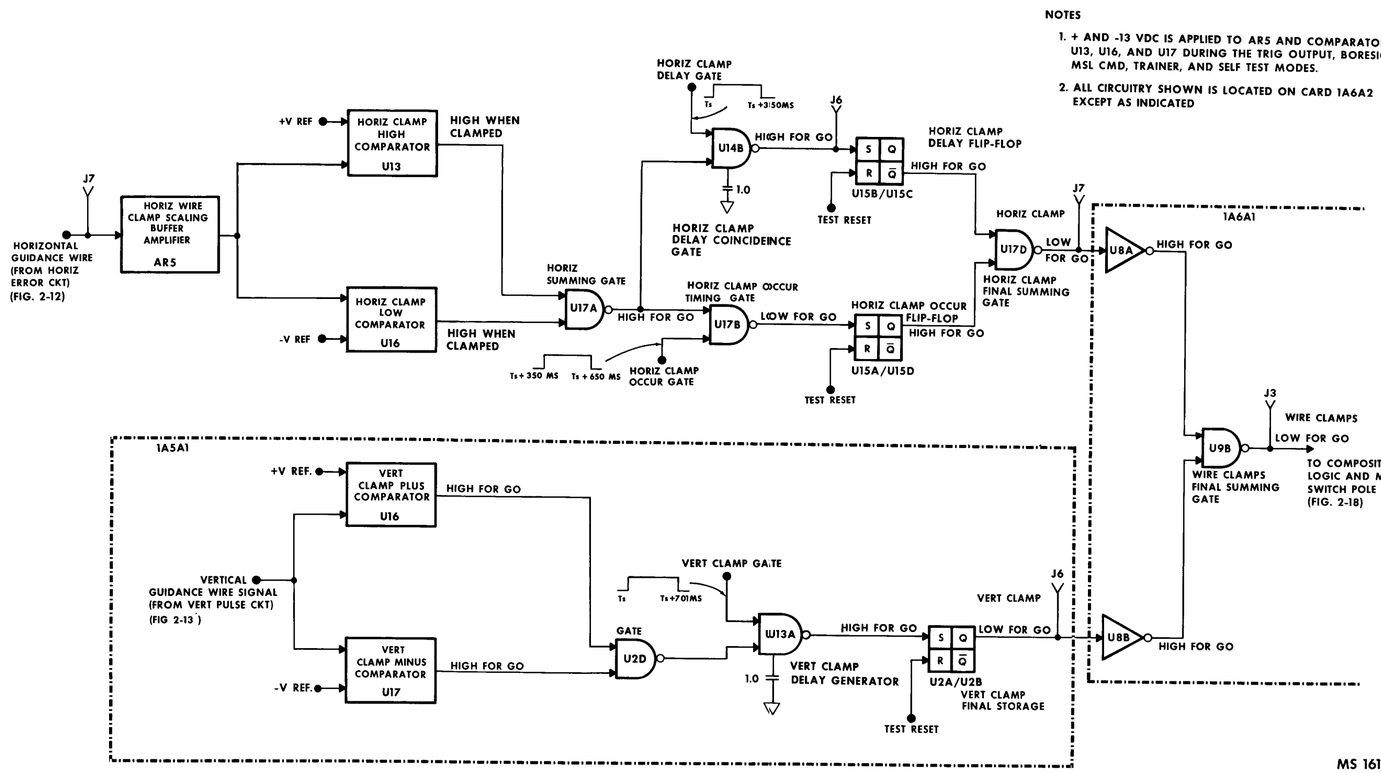

Figure 2-11. Horizontal and vertical wire clamp evaluation - functional block diagram

(a) The horizontal guidance wire signal from the UUT is routed to AR5 on 1A6A2. Amplifier AR5 has a gain of 10.5. The output of AR5 is coupled to U13 and U16, the horizontal clamp high and low comparator. If the input signal to AR5 is within the ±0.500 volt level, the outputs of U13 and U16 will be high. These two outputs are checked by U14B from Ts through Ts +350 msec to insure the horizontal wire is clamped during this time. In addition, the outputs of U13 and U16 are checked again from Ts +350 msec through Ts +650 msec to insure that the horizontal wire signal is now unclamped, and is receiving some error information.

(b) The vertical guidance wire signal on card 1A5A1 is coupled to U16 and U17 on 1A5A1 after being buffered by AR1 on 1A5A1. If the input to U16 and U17 (the vertical clamp plus and minus comparator) is within the ± 0.500 volt level, the outputs of U16 and U17 will both be high. If the output of U2D remains low during the period from Ts through Ts +701 msec, the output of U13A will remain high (go state) and the output of memory circuits U2A/U2B will remain low for a go.

(6) The ripple test is performed in both the boresight and missile command modes. In this test, the TTS insures that the UUT peak ripple, which is a tracker horizontal guide wire generated signal, has a minimal peak value of 86 MV and a maximum peak value of 662 MVdc.

(a) The circuitry is located on card 1A6A2 and is shown in figure 2-12. The ripple on the UUT horizontal guidance wire is removed from its dc carrier by capacitors C6 and C8 on card 1A6A2. The ripple component is amplified by AR4 and then fed to voltage comparators U6 and U10. Comparator U6 switches at 662 MV peak and comparator U10 switches at 90 MV peak.

(b) When the horizontal guidance wire ripple exceeds 90 MV peak U10 output switches high and U8B and U8C output switches high which enables the horizontal error evaluation logic U9A and produces a low at U9B output. The ripple test is initiated concurrently with the horizontal error test from Ts +12.0 seconds through Ts +13.0 seconds.

(c) If the input ripple exceeds 662 MV peak, U6 output will go high causing the U9B output to go high for a system no-go.

(7) The horizontal error test is performed in both the boresight and missile command modes. The ripple evaluation circuit is shown in figure 2-12 and described in the preceding paragraph. It enables the horizontal error evaluation circuit when the ripple peak value is greater than 90 MV and less than 662 MV.

(a) In the foresight mode the TTS evaluates the UUT horizontal guidance wire dc voltage component while the UUT IR Detector is in line of sight with the OAC IR

diode (boresight condition, ≃ zero position error). Any horizontal position error in the boresight alignment is seen as a plus or minus voltage on the horizontal guidance wire. With the above IR stimuli the TTS verifies that the position error voltage (difference in alignment between the OAC and UUT) on the UUT horizontal guidance wire output is zero ± 824 MVdc. The exact voltage is sampled and stored for use as the reference voltage in the missile command test mode.

(b) In the missile command mode the OAC IR source is offset from center of the UUT detector cell by 2.36 MR left and 2.36 MR down. The horizontal component of this IR offset is seen as a plus dc voltage on the UUT horizontal guidance wire. This horizontal guidance wire dc voltage is compared with the dc voltage stored during the boresight mode test. The TTS verifies that this voltage is between +3.77 and +5.15 Vdc for a go condition.

1. The circuitry for this test is located on card 1A6, A1 and A2 sides and is shown in figure 2-12. The UUT horizontal guidance wire signal is filtered by the AR1 circuit on 1A6A2. In the foresight mode voltage comparators U1 and U2 outputs will be less if the sample voltage is between -824 and +824 MVdc giving a low at the output of U9A. The output of AR1 is also fed to and stored on the boresight horizontal error storage capacitor for use as a boresight reference voltage in the missile command test mode.

2. In the missile command mode the horizontal error filtered voltage is compared by AR3 with the stored reference voltage on the boresight horizontal error storage capacitor 1A6A2-C3. The amplified output of AR3 will produce a high at the U3 and U4 output if the AR1 output is between +3.77 and +5.15 Vdc. This will result in a go condition (low) at U9A output.

(8). The vertical pulse (figs. 2-11 and 2-13) test is performed between Ts and Ts +13 seconds to verify that the UUT vertical pulse, on the vertical guidance wire, has a minimum amplitude of +7.9 Vdc and a minimum pulse width of 9.0 msec at the +5.0 Vdc amplitude level of the pulse. This test also verifies that the first vertica guidance wire pulse occurs within 701 to 749 msec after Ts.

(a) The UUT vertical pulses are received in buffer amplifier AR1 on card 1A5A1 and then routed to voltage comparators U7, U9, U16 and U17. Pulse width comparator U9 stimulates the pulse width and pulse repetition rate circuits. The U9 output is low until a vertical pulse is applied to its input. When the input pulse voltage exceeds the +5 Vdc threshold of U9, the U9 output goes high. When the input pulse voltage falls below +5 Vdc, the U9 output goes low. This action produces a pulse out of U9, the width of which is equal to the time the input pulse is

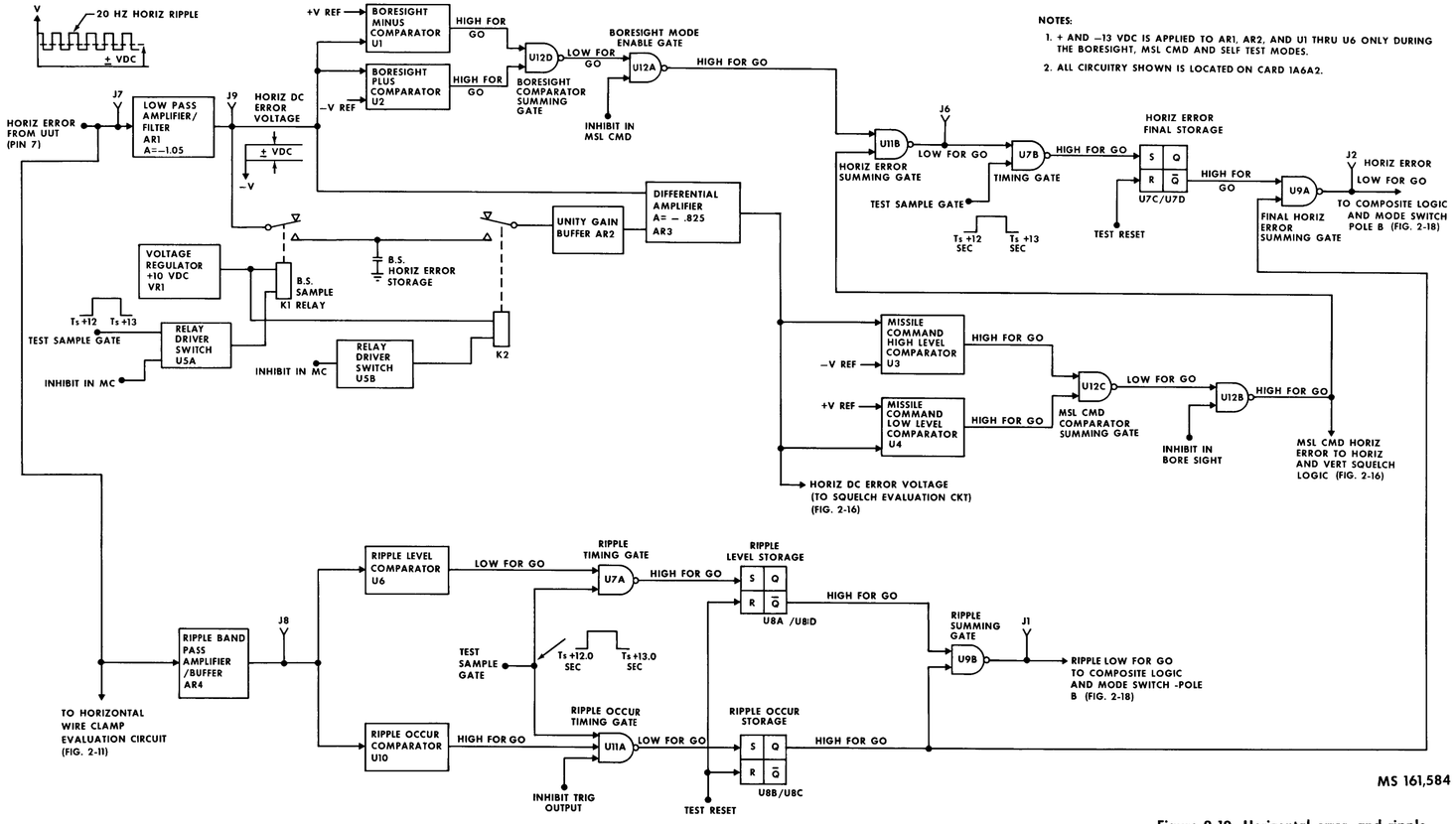

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Figure 2-12. Horizontal error, and ripple evaluation - functional block diagram.

NOTES

1. + AND - 13VDC IS APPLIED TO AR1, U7 AND U9 ONLY IN THE BORESIGHT, MSL CMD AND SELF TEST MODES
2. ALL CIRCUITRY SHOWN IS LOCATED ON CARD 1A5A1
3. TIME INDICATED AS X IS THE LEADING EDGE OF EVERY VERTICAL PULSE, W IS THE TRAILING EDGE

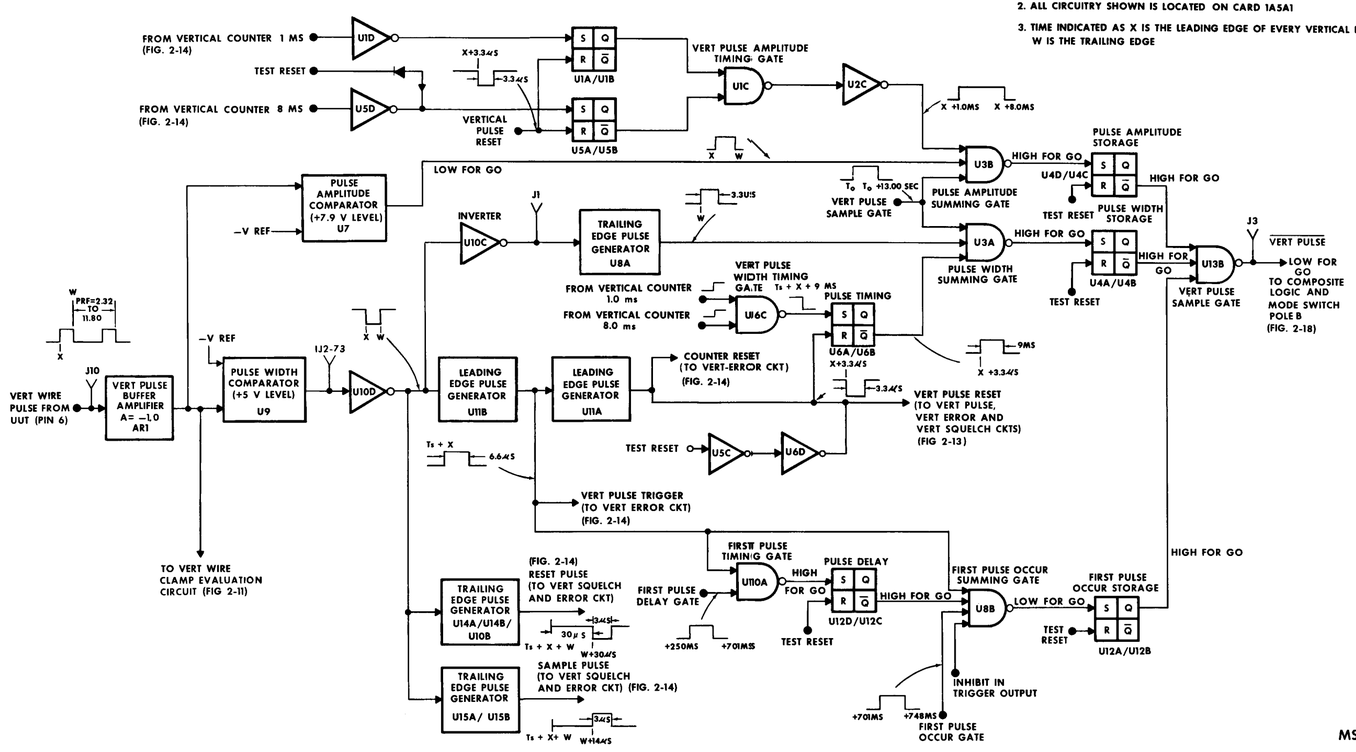

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Figure 2-13. Vertical pulse evaluation- functional block diagram

greater than +5 Vdc. The time when U9 output goes high will be considered the leading edge of each vertical pulse or time X while the trailing edge will be the U9 output return to a low, and time W. U9 output will then be high for the period x + W (vertical pulse width). This pulse will be inverted by U1OD and applied to leading edge pulse generators and trailing edge pulse generators. Leading edge pulse generator U11B developes a pulse which goes high with the leading edge of the input pulse and remains high for 6.6 µS. This vertical pulse trigger is applied to the first pulse evaluation circuit. The first vertical pulse should not occur between Ts +250ms and Ts +701 ms. The first pulse delay gate applied to U10A is high from Ts +250 ms to Ts +701 ms. If a vertical pulse trigger applied to U10A occurs during this time U10A output would go low setting pulse delay flip-flop U12D/U12C. This would produce a low for no-go. If no vertical pulse occurs during this time, U10A output remains high and U12D/U12C remains reset providing a high for go. U12D/U12C output, a vertical pulse trigger and the first pulse occur gate which is high from Ts +701 ms to Ts +748 ms is applied to U8B. The vertical pulse trigger should go high during this time producing a low from U8B. This low would set U12A/U12B providing a high for go. This indicates no pulse before Ts +701 ms and a pulse occurring between Ts +701 ms and Ts +748 ms. The output of U11B is high for 6.6 µsec from the leading edge of each vertical pulse to develop the vertical pulse trigger. This output is coupled to U10A. The first vertical signal pulse should not occur until the first pulse delay gate occurs from Ts +250 msec through Ts +701 msec. If the vertical does not occur in this period, the inputs to U10A should not be in coincidence, and the output of U12D and U12C should remain high. With the occurrence of the first pulse occur gate and receipt of the first vertical pulse from U11B, all inputs to U8B should be high, resulting in a low at the output of U8B for go. This insures that the first vertical pulse is occurring at the proper time.

(b) Nine msecs after the leading of each vertical pulse, both inputs to U6C will be high, resulting in a low to the set input of U6A and U6B. This will produce a high output from the U6A/U6B flip-flop at X +3.3 µsec for a period of 9 msec. This 9 msec period provides a test window to U3A. The trailing edge of each vertical pulse is used to trigger U8A, providing a high output at time W for a period of 3.3 µsec. All inputs to U3A will be high if the vertical pulse width is less than the 9 msec window. This condition will result in a low (no-go) output from U3A. However, if the vertical pulse width exceeds 9 msec (go), the output of U3A will remain high for go.

(c) The output of AR1 is taken to the pulse amplitude comparator U7. If the amplitude of each vertical pulse exceeds the +7.9 volt trip level of U7, the output of U7 will be a low. This output is coupled to U3B, and summed with the 7 msec test window out of U2C. The output of U3B should remain high for go.

(9) The vertical error (fig. 2-14) test is performed in both the boresight and missile command modes from Ts +12.0 through Ts +13.0 seconds. In the boresight mode, when an IR boresight stimulus (this refers to the IR stimulus input into the UUT detector on a boresight line of sight) is applied to the UUT, the TTS verifies that the UUT vertical guidance wire pulse repetition rate on the UUT vertical guidance wire is between 2.32 and 3.28 pulses per second (PPS). The TTS measures the vertical guidance wire repetition rate by determining the time between each pulse pair which occurs during a 1.0 second sample gate (Ts +12.0 to Ts +13.0 sec.). This monitor circuitry is located on card 1A5 of the TTS monitor unit. In the missile command mode when the UUT and the OAC are aligned to the missile command error (2.36 MR down and 2.36 MR left) point, the vertical component of this offset is seen above the nominal repetition rate on the UUT vertical guidance wire. The TTS verifies that the UUT vertical guidance wire pulse repetition rate is between 5.78 and 11.80 PPS. The missile command measurements are made on the same manner as the boresight.

(a) The binary coded decimal (BCD) counters U1, U2, U3 and U4 are triggered by a 10 kHz master clock pulse. The counter is reset by the leading edge of each pulse on the vertical wire. This reset lasts for 3.3 μsec.

(b) With both inputs to U17D high from 304.8 to 431.0 msec after the leading edge of each vertical pulse, a low output will result. With one input to U17C high (during boresight) and one input low, at 304.8 msec after the occurrence of each vertical pulse, a high will result to the input of U22B. U24B is inhibited during boresight, producing a high output, which is coupled to the input of U22B. When the next vertical pulse occurs, if it is in the detection window period of 304.8 msec to 431.0 msec after the previous pulse (2.32 to 3.28 PPS), all inputs to U22B will be high, generating a low for go output. The same function occurs during the missile command mode, except U24A and U24B are utilized, checking for a vertical pulse repetition rate of 5.78 to 11.80 PPS (detection window period of U24A is from 84.8 msec to 173msec). The vertical error status is then stored by flip flop U24D/U24C.

(c) The sample pulse at the input of U25B occurs at 14 μsec after the trailing edge of each vertical wire pulse. This 3 μsec pulse arms U25B. This provides a window for checking the output of U24D and U24C. A reset pulse is generated

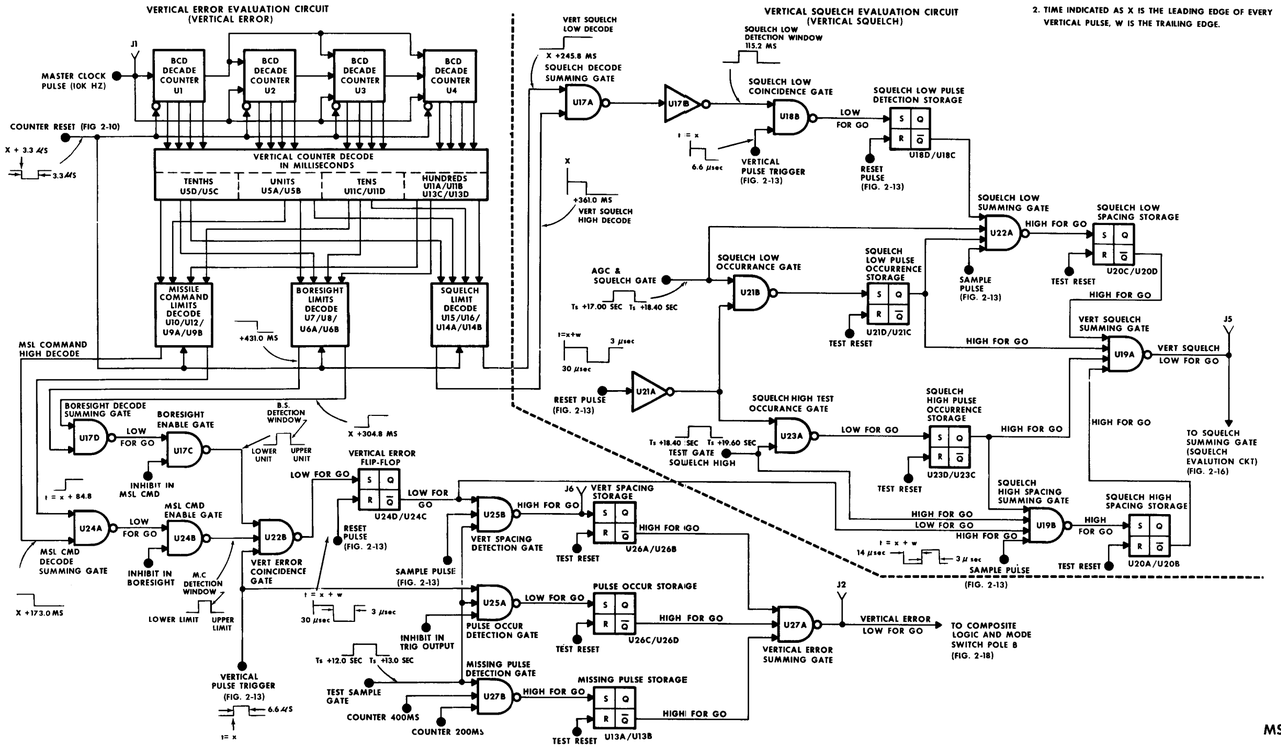

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Figure 2-14. Vertical squelch and vertical error evaluation - functional block diagram.

30 μsec after the trailing edge of each vertical wire pulse and is used to reset U24D and U24C.

(d) The missing pulse detection gate receives counter inputs at 200 msec and 400 msec after the counter has reset from the leading edge of a vertical pulse. These two inputs will be high together at 600 msec after X. The next reset pulse will occur with the leading edge of the next vertical pulse. If any vertical pulse reset is absent, all inputs to U27B will be high at 600 msec (during the test time), resulting in a low for no-go output. If every vertical wire pulse occurs within 600 msec of the prior pulse, the 200 msec or 400 msec inputs will be low, resulting in a high output from U27B.

(10) In the boresight and missile command modes the TTS verifies that the maximum safe impedance (of a safed UUT trigger) is 205 mil ohms. This test is performed by the trigger safe (fig. 2-15) dc level test circuit on card 1A7A1. The TTS also verifies that the impedance of a series RL network (605 μh and 300 mil ohms in parallel with a 3000 pf capacitor) simulates a UUT unsafe trigger switch and provides a no-go condition. This test is performed by the trigger safe transient test circuit on card 1A7A1. The evaluation is performed by the TTS at Ts +19.6 to Ts +21.0 seconds when a constant current pulse is fed from card 1A7 to the trig output, pin 15 on the UUT, and back through power ground pin 14. The voltage drop across the trigger resistance in parallel with OAF trigger load resistor is fed back to card 1A7 and is evaluated as a go or no-go.

(a) An output of 250 ma dc from the constant current generator AR2, Q1, Q2, Q3, and VR2 is passed through the UUT trigger safe circuit in parallel with the OAF load resistor to ground. The voltage drop developed across the OAF load resistor is coupled to TTS differential amplifier AR1 on card 1A7A1. This differential amplifier has a gain of 20 and the output is connected to voltage comparator U1 and U2. If the trigger safe voltage drop is within limits, the output of U2 will be low to the input of U9B. U9B is armed 140 μsec after a current step is initiated. This 140 μsec delay allows the AR1 output to stabilize so that a pure resistive reading may be evaluated.

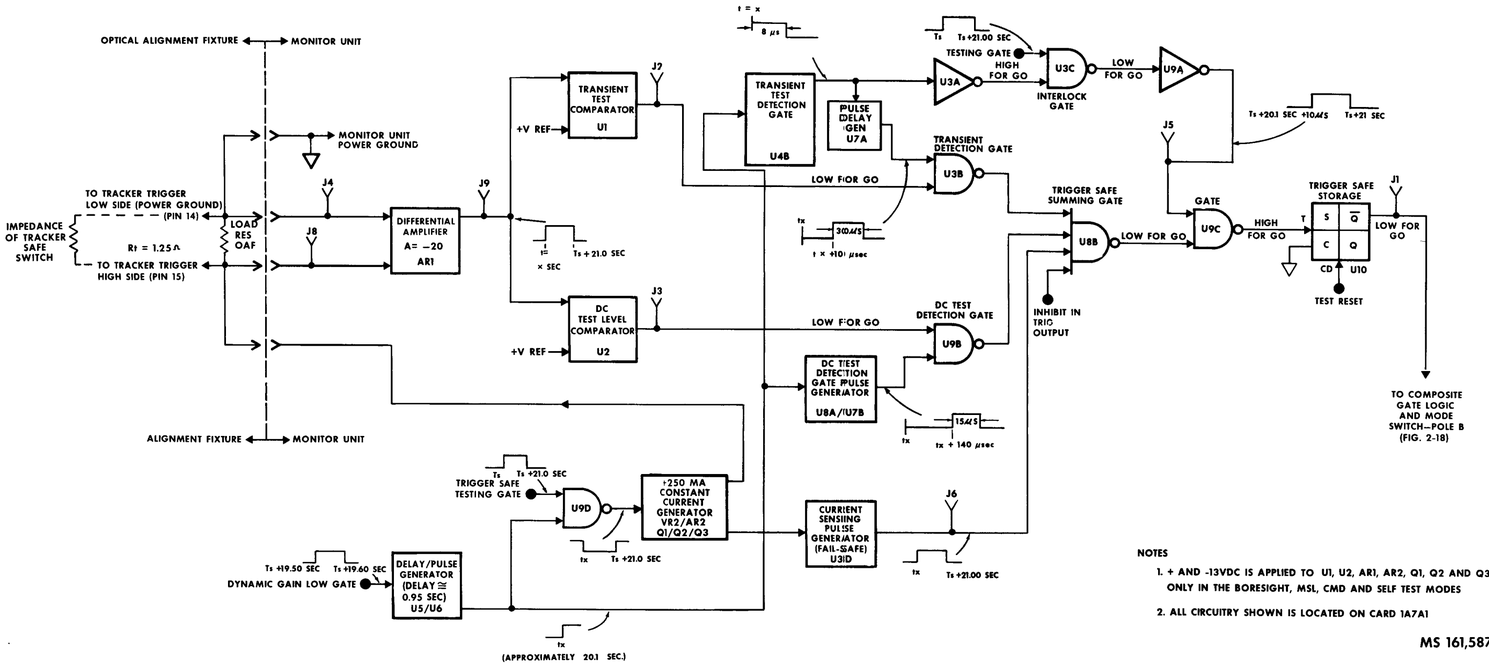
(b) If the UUT trig safe circuit is inductive, due to a faulty UUT trig safe switch, ($\geq$ an equivalent of 605 μh and 300 mil ohms in parallel with a 3000 pf capacitor), then the current step through the parallel combination will instantaneously develop a voltage spike which will decay after some time constant. If this transient is > 200 mVdc at the output of AR1 then U1 output will switch high. Also this spike must occur within 10 to 40 μsec after the current step is initiated.

If so, U3B output will switch low for a transient test no-go.

(11) The squelch test is performed in the missile command mode from Ts +18.4 through Ts +19.6 seconds. During the squelch evaluation test, the emitting IR diode excitation is reduced 85 percent, while the vertical wire, horizontal wire, vertical rate position and horizontal rate position signals from the UUT are monitored. The squelch evaluation circuitry verifies that the horizontal wire dc level does not deviate more than ± 15 percent from the pre-squelch dc level during the period of squelch. The vertical wire is monitored during the squelch period for a pulse repetition rate between 2.77 and 4.07 PPS. At the completion of the induced UUT squelch period, the monitor unit verifies the horizontal wire dc level returns to the pre-squelch point and the vertical wire pulse repetition rate returns to the pre-squelch rate. The horizontal and vertical rate position parameters are monitored during squelch to verify no false samples occur.

(a) In the horizontal squelch circuit (fig. 2-16) the horizontal error signal is taken from the output of AR3 on card 1A6A2 and fed through K2 on 1A6A1 to the horizontal squelch sample and hold amplifier (AR3). AR3 detects the pre-squelch condition of the horizontal guidance wire signal from the UUT and stores this value. At Ts +16.8 seconds, K2 energizes, removing the signal from the input of AR3. The squelch horizontal wire voltage is now compared with the reference out-of-squelch voltage stored by AR3, by high and low comparators U1 and J3. If the horizontal dc in-squelch voltage is within 15 percent of the out-of-sight dc voltage, the outputs of U3 and U1 will switch to high for go. When the IR squelch level is removed at Ts +18.4 seconds, the horizontal error shall return to the pre-squelch value. If the horizontal wire error voltage is within 3.77 and 5.15 Vdc, a high for go will be felt at the output of U12B and to the input of U6D. A low (no-go) at the input of U6D will result in a high (no-go) at the output of U9A. With the TTS in this mode, a horizontal error no-go will produce a squelch no-go indication.

(b) In the vertical squelch circuit, the vertical pulse trigger is coupled from the output of U11B (fig. 2-13) to U18B (fig. 2-14). The input to U18B is derived in the following manner: BCD decade counters U1 thru U4 are driven by the master clock 10 kHz pulse. Time outputs of 200 msec, 40 msec, 4.0 msec, 1.0 msec, and 0.8 msec are coupled to the input of squelch low limit decode U14B and U15. These inputs generate a high output from U15 at 245.8 msec (the combined value of each of the timed inputs). Time outputs of 300 msec, 40 msec, 20 msec and 1.0 msec are fed to the inputs of squelch high limit decode U14A and U16. These inputs



NOTES

1. + AND −13VDC IS APPLIED TO U1, U2, AR1, AR2, Q1, Q2 AND Q3 ONLY IN THE BORESIGHT, MSL, CMD AND SELF TEST MODES

2. ALL CIRCUITRY SHOWN IS LOCATED ON CARD 1A7A1

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Figure 2-15. Trigger safe evaluation- functional block diagram

NOTES

1. ALL CIRCUITRY SHOWN IS LOCATED ON CARD 1A6A1
2. + AND -13VDC IS APPLIED TO AR3 IN THE TRIG OUTPUT, BORESIGHT, MSL CMD, TRAINER, AND SELF TEST MODES

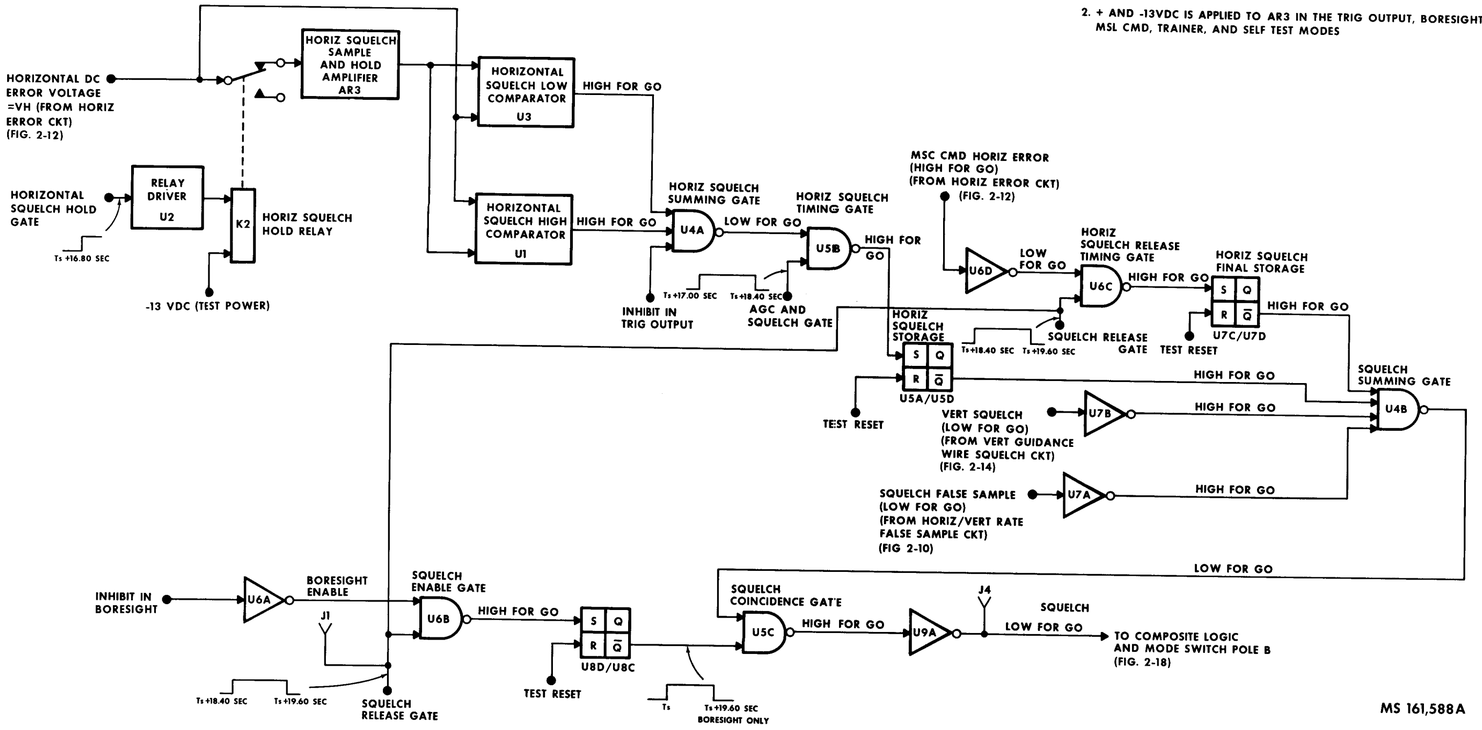

Figure 2-16. Horizontal squelch evaluation-functional block diagram

generate a low output from U16 at 361.0 msec. This produces a high to both inputs of U17A for a period of 115.2 msec, causing a high to the input of U18B. All BCD counters (fig. 2-14) are reset with the leading edge of the vertical pulse (time X). The 115.2 msec high to U18B will occur from X +245.8 msec thru X +361 msec. If the leading edge of the next vertical pulse occurs during this 115.2 msec window (2.77 to 4.07 PPS), both inputs to U18B will be high, generating a low for go output from U18B. This circuitry, through U22A, checks out the vertical pulse repetition rate during an in-squelch condition. During the squelch period, U22A and U19A are armed by the logic gates U21D/U21C, U21B and U21A. At the completion of the squelch period (Ts +18.4 to 19.6 sec.) gate U23A output goes low and U21B output goes high which disarms U22A and arms U19B. If the vertical guidance wire repetition rate is between 5.78 and 11.80 PPS (pre-squelch level) the U24D/U24C flip-flop output will be low for go. This is passed by U19B and seen as a low at the output of U19A.

(c) The squelch false sample circuit is shown on figure 2-10. During the squelch period (Ts +17.0 to 18.4 sec.), the false sample monitor portion of the circuit is armed by coincident gate U19C on card 1A10A1. If no false samples occur U10C output will remain high and the output will be seen as a low at U9B output.

(d) The test functions described in the above steps are summed by the squelch summing gate U4B on card 1A6A1 (fig. 2-16).

(12) The trigger output system (fig. 2-17) evaluates the UUT trigger output energy envelope during the trigger actuation. The test verifies that the trigger output energy is greater than 17.0 mil joules and that the pulse duration is equal to, or less than 10 mil sec. The test is performed by firing the UUT trigger into a load resistance in the OAF. The total resistance of the load is calibrated to 1.25 ohms. The total load consists of wire resistance, contact resistance, and a resistor combination.

(a) When the UUT trigger (fig. 2-17) energy envelope is fed into the TTS load resistance, a voltage drop is developed across sense/resistor R4 in the OAF. The voltage level developed across R4 is fed to the differential amplifier AR1 on card 1A7A2 for evaluation. The AR1 (gain -2.74) differential amplifier output on card 1A7A2 is then squared, by U1 and integrated by AR2. The timing circuit for the pulse width is initiated by the AR1 output. This output is fed to voltage comparator U2. This (U2) comparator will switch when the input level (to AR1) exceeds 117 mil volts which will arm gate U3D allowing the trigger output timing pulse to activate switch U4. The U2 output on 1A5A2 is also fed through U3C and flip flop

(U8A/U8B) to arm (high) U8C, allowing the 10 KHz pulse to be fed through to U9 and U10 (10 KHz comes from the master counter on card A4). The purpose of U9 and U10 is to produce an 8 ms pulse which switches flip flop U7 when the TTS mode switch is in trigger output (enables U3A output [Hi]). The output is a 10 msec pulse which is fed to gate U3D.

(b) The output of U3D will be low as long as the input pulse (to AR1) is still above 117 mVdc and if the time period is less than 10 msec. As soon as the input pulse decays, the voltage comparator U2 will switch low and U3D will switch high. If the 10 msec timing pulse times out before the trigger pulse decays, the U3D output will switch high. The positive pulse from U3D switches U4. When U4 switches, a ground is fed to the AR2 integrator which stops integration and returns the integrated pulse to zero. The integrated pulse amplitude is fed to the voltage comparator U5. If the trigger output pulse is greater than 17 mil joules and $\leq$ 10 msec wide the U5 output will switch low and then be stored by U6. The trigger output status is fed out through pin 8 of card A7.

(c) In summary, the integrator will continue to integrate for the pulse width or until 10 msec has elapsed. The voltage height of the integrated output is fed through the U5 peak detector for a final status.

(13) Outputs from the evaluation circuits (fig. 2-18) are coupled to the composite logic where the inputs are inverted, summed, inverted again, and fed to a final composite summing gate. When the mode switch is in the boresight or missile command position, the output of the composite summing gate is connected to the input of the lamp readout logic. The monitor unit indicator lamps will display the status of the UUT. If the condition displayed is a go in boresight or missile command, then all sub-mode evaluation outputs must be in a go state. However, in the trigger output position, the composite gate logic is not used and the go or no-go status is coupled directly to the lamp readout logic. When in one of the five primary modes of operation, certain other functions are inhibited (placed at ground or low condition). This inhibit function is performed by the mode select switch.

g. Self-Test and TTS Monitor Function. When the mode switch is placed to self-test, and the test start/stop switch momentarily depressed, a timed 60-second self-test of various circuits of the TTS is induced. This self-test may be conducted with or without a UUT installed. Load resistors are switched across outputs of the power supplies to simulate UUT nominal loads. During the 60-second self-test period, the monitor select switch is rotated and the operator may display on the

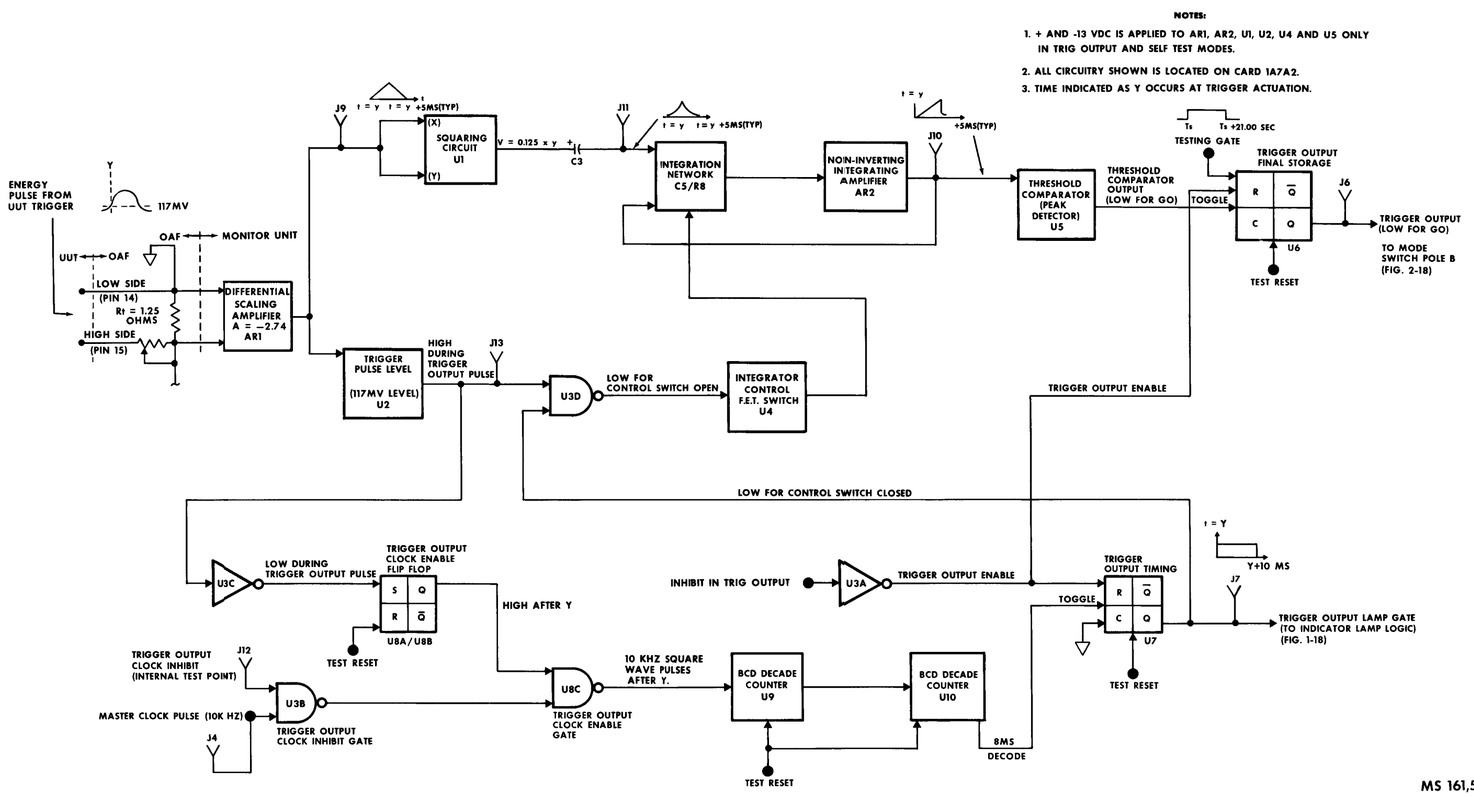

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Figure 2-17. Trigger output evaluation - functional block diagram.

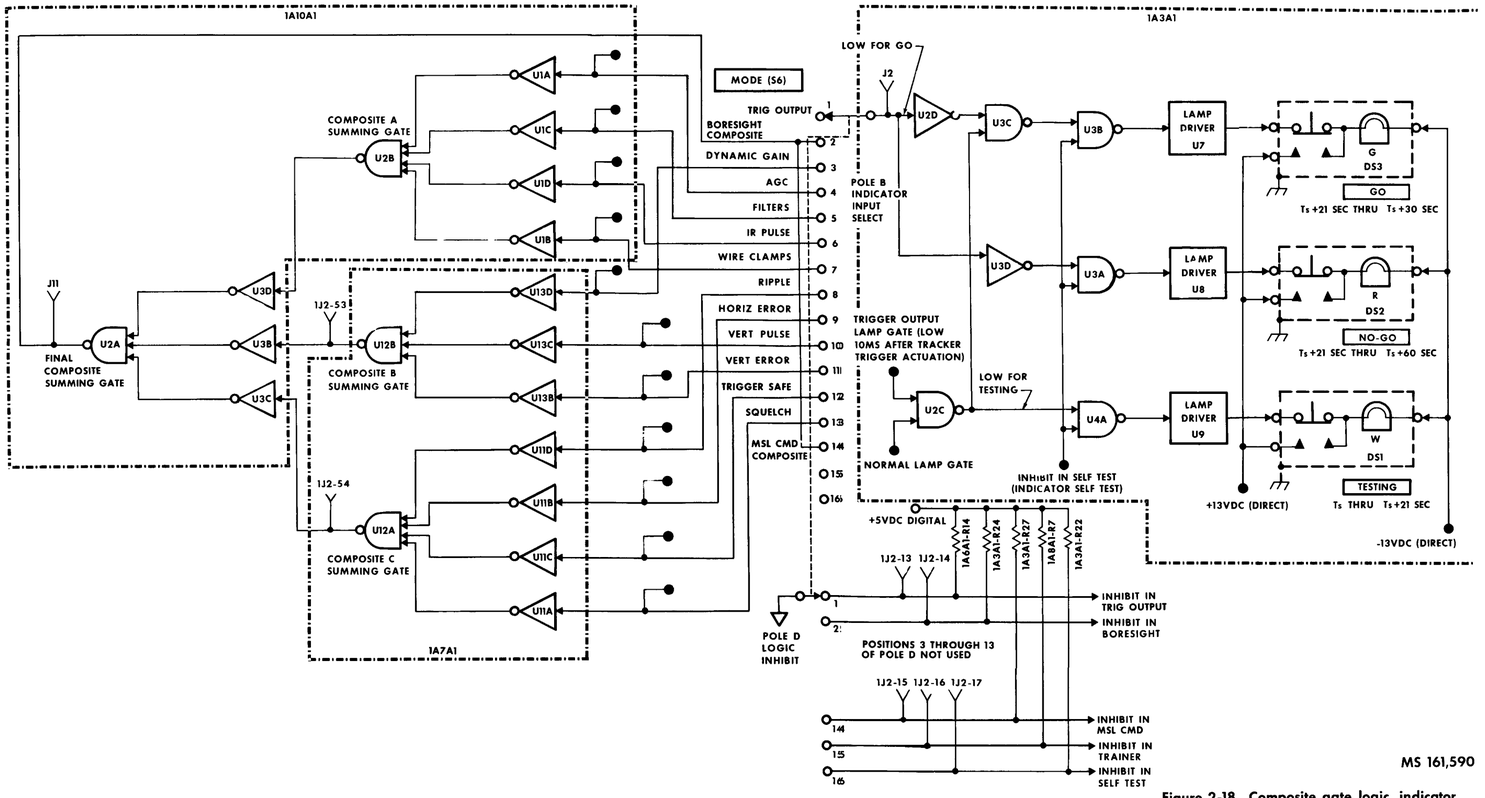

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Figure 2-18. Composite gate logic, indicator readout logic and logic inhibit function - functional block diagram

monitor meter the charge status of the monitor unit batteries, the ± 5.0 Vdc reference voltage, the +5.0 Vdc digital, and the IR output.

(1) With the mode switch placed in self-test, the relay actuate diode matrix on 1A2A1 (fig. 2-5) actuates 1A6A1-K1, shorting power ground to signal ground. Relay 1A2A2-K1 is also energized, applying load resistors R1 and R2 across the TTS power supplies.

(2) With the monitor select switch in positions 1 through 6, the respective outputs monitored are depicted in figure 2-19.

(3) When the monitor select switch (fig. 2-19) is in the +batt A, +batt B, -batt A, and -batt B positions, the positive battery voltage is connected through pole A and the energized contacts of 1A9A1-K1 to 1A9A1-AR1. The negative battery voltage is connected through pole B and the energized contacts of K1 to AR1. The output of AR1 triggers relay driver 1A9A1-Q1, energizing K2. When K2 energizes, the output of AR2 is connected to the negative terminal of monitor meter Ml. The input to AR2 is from the thermistors located on the battery pack. These thermistors are connected in the feedback circuit of AR2, and tend to regulate the gain of AR2. The output of AR2 is adjusted to -8.62 Vdc @25°C (77°F). With K2 energized, the monitor series scaling circuit is bypassed and the output from AR2 is connected directly to M1. The positive terminal of M1 is connected to the output of AR1. This output is from +7.0 to +12.0 Vdc over the operating temperature range.

h. Time Sequence Generator and Decode (fig. 2-20). The time sequence generator contains the master clock 20 kHz oscillator, a divide-by-two symmetry flip-flops and six BCD decade counters. These counters provide the time outputs necessary to produce the various gates for the TTS. The time sequence decade consists of the logic used for generation of these timed gates, and provides output of the timed gates to circuitry of the monitor unit. The time sequence decade inputs are produced by the time sequence generator. All counters are reset to Ts when the test reset inputs go high. When the TTS is operated in the trainer mode, the 10 kHz master clock is inhibited after Ts +4.0 seconds, and no timed outputs are produced by the time sequence generator. The output of U6B goes low at this time to clear the data input to U15, stopping the clock output.

i. LET Signal Simulation. When the TTS is connected to the LET and the trainer trigger switch is depressed, two output signals are generated from the TTS to simulate actual operating conditions of the UUT and the round. One signal is the simulated UUT trigger pulse which starts the UUT program. The second output is a

280 mVac 5.0 kHz sinowave to the sum signal monitor input of the UUT. These signals are generated as follows:

(1) When the TTS trainer trigger switch (fig. 2-21) is depressed, a ground is placed on the schmidt trigger input U2 and card 1A8A1 causing the output to pulse high. The falling edge of this pulse makes the flip flop U1 output switch high. In any mode except trainer, the U3 output is low. This U1 output step is fed through the pulse forming network in cable 10278398 to the LET.

(2) The output of U1 on 1A8A1 is also fed to card 1A10A1 to arm U6A. This allows the trainer frequency stimulus square wave to be shaped and amplified by the AR1 circuit. The output of this circuit is fed through the LET to the MTS.

j. Optical Alignment Fixture (OAF). The OAF provides for mechanical mounting of the UUT and the OAC for tests of the UUT and for operation with the LET and MTS. The OAF houses card 2A1, containing the IR source current generator and IR source control logic. Card 2A1 also contains a lamp voltage regulator circuit (VR2 and VR3) which, in conjunction with the three lamp controls on the OAF, allow the intensity of the collimator self-test and reticle lamps and the tracker reticle lamp to be turned on or off and the intensity varied.

k. Optical Alignment Collimator (OAC). The OAC consists of cylindrical metal housig containing two IR source diodes (near-center CR1, and off-center CR2), a source lens assembly, an eyepiece lens assembly, and objective lens assembly. An IR detector diode CR3 is located within the OAC and is used for monitoring and self-test of the IR source diodes. The OAC must be placed on the OAF to provide an IR stimuli for the UUT. The functions of the diodes, thermistor, and card 3A1 are discussed in para. 2-2e. The following functions are depicted in fig. 2-22.

(1) The modulated, intensity-controlled, collimated, IR stimuli are produced by either CR1 or CR2.

(2) The source lens assembly receives and directs the light sources within the OAC.

(3) The collimator cell assembly contains the collimator reticle; it provides the alignment markings and scales used during UUT and OAC alignment and operational evaluation of the LET and MTS.

(4) Illumination of the OAC for adjustment and alignment is provided by the reticle and self-test lights. Intensity of the lights is variable from off to a maximum by controls located on the OAF.

(5) Thermistor RT1 is mounted on CR1 compensates for temperature sensitivity.

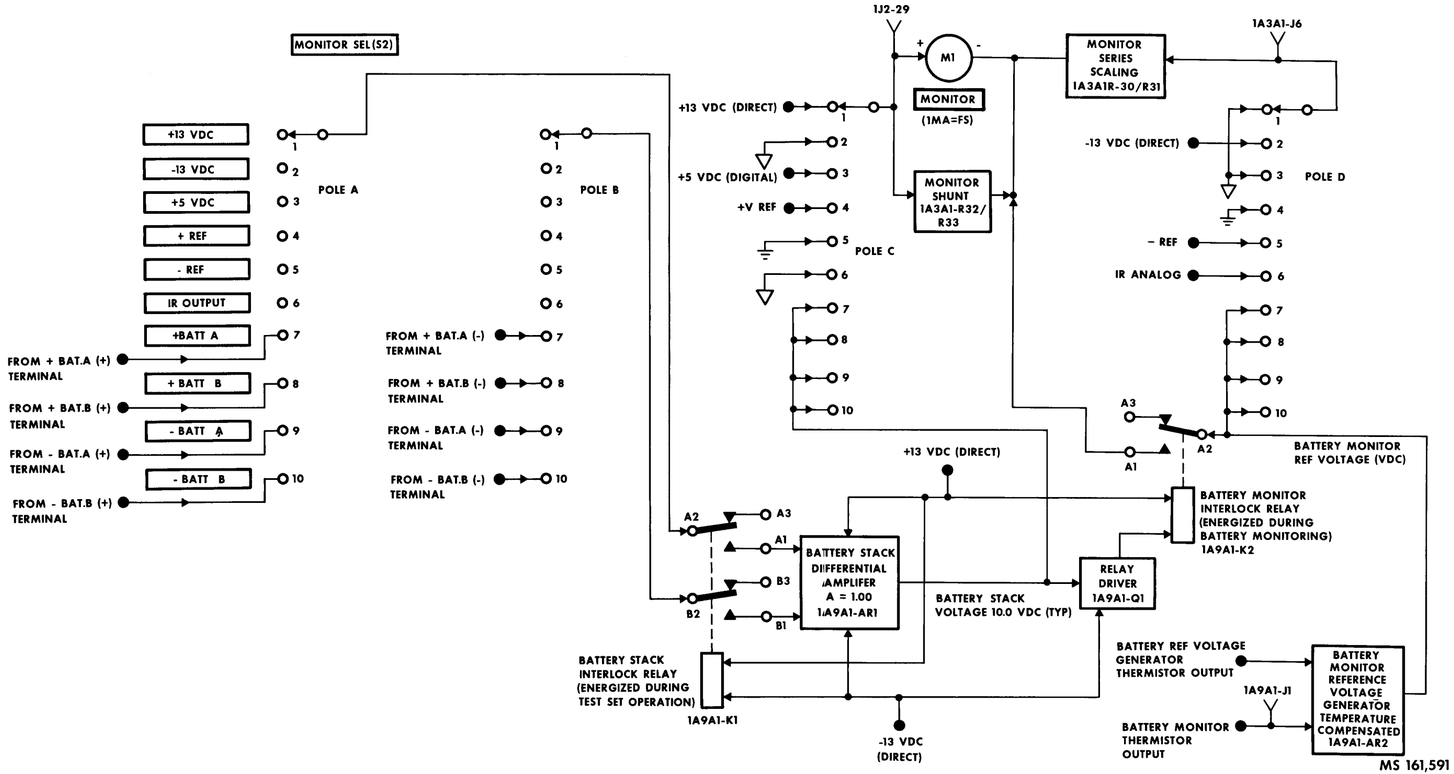

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Figure 2-19. Tracker test set monitor function - functional block diagram.

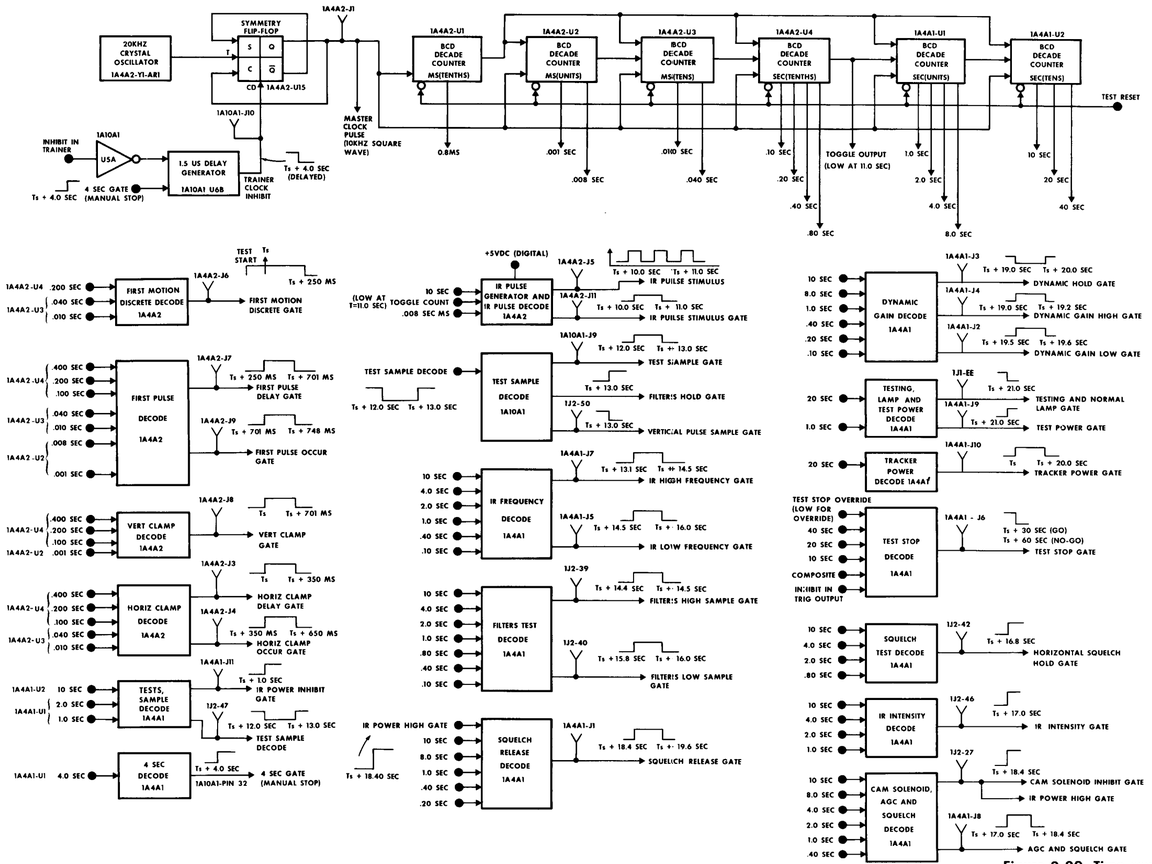

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Figure 2-20. Time sequence generator and decode - functional block diagram.

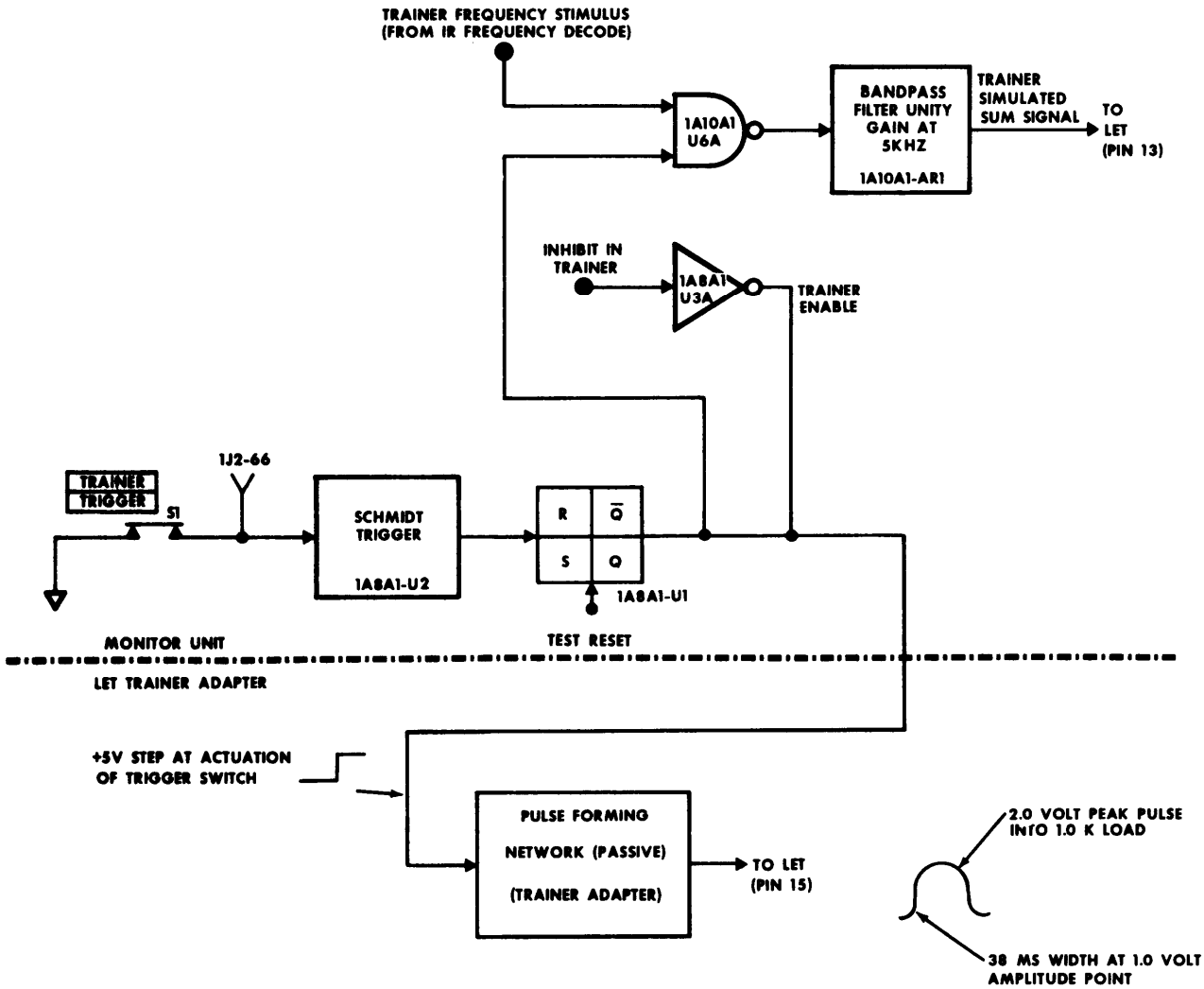

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Figure 2-21. LET signal simulation - functional block diagram.

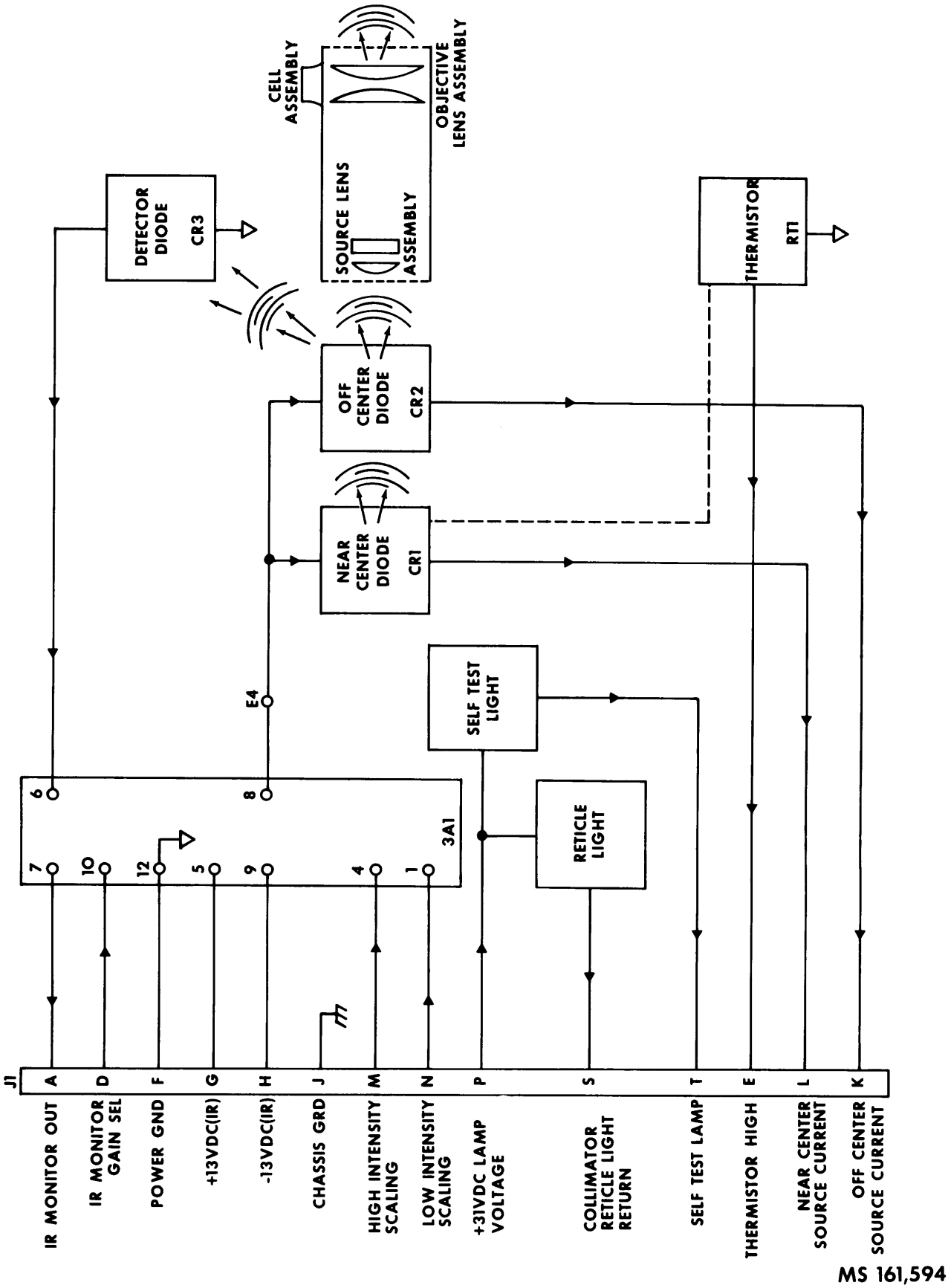


Figure 2-22. Optical alignment collimator - functional block diagram.

Output of the thermistor is coupled to the IR source dc reference generator on card 1A8A1 and IR monitor on card 1A9A2.

2-3. Mechanical and Optical Functions.

a. The OAF (fig. 2-23) provides a common mounting platform for the OAC and the UUT. The OAC guide pins position the OAC for seating in the collimator mount. Locking controls are provided on the collimator mount securing the OAC to the mount and retaining it in position. The collimator guide is connected by mechanical linkage to the azimuth and elevation adjustment knobs. These adjustments provide smooth linear movement of the OAC for precise alignment with the UUT in both axes. The UUT mount provides for mechanical mating and contains the connector, allowing interface between the UUT and TTS. When the UUT is inserted in the mount and pushed to the rear, the UUT latch secures and retains this position. Two UUT positioning slides provide quick, easy UUT alignment.

b. The OAC optics are depicted in figure 2-24.

(1) The source lens assembly receives and directs the light sources within the OAC. The beam splitter projects the visible light from the UUT reticle backlight and from the collimator reticle and self-test lamps. The deflected light from the beam splitter is directed upon the eyepiece cell assembly.

(2) The eyepiece cell assembly provides a reticle that permits viewing the UUT reticle with respect to the collimator reticle. Incandescent lamps are used to backlight the OAC and UUT reticle during boresight and missile command alignment. The visible light is passed through the collimator cell assembly to the eye lens. The focusing ring surrounding the eye lens permits the operator to obtain clear and sharp focus of OAC and UUT retitles during the alignment procedures.

(3) The IR signal is passed from the source lens assembly, through the field correction lenses, through the OAC, to the objective lens. Collimated IR energy is passed through the objective lens to the UUT. The objective lens assembly is equipped with a focus control which enables the operator to adjust the focal length of the OAC to compensate for changes in environmental conditions.

c. The tetrahedral prism consists of a housing shaped to fit on the forward end of the OAC and encloses a corner cube prism assembly. The prism, when mounted on the front end of the OAC, is used by the operator to check the internal alignment of the OAC. The prism intercepts the visible self-test light source from the OAC, and reflects the beam onto the eyepiece reticle of the OAC. The reflected light

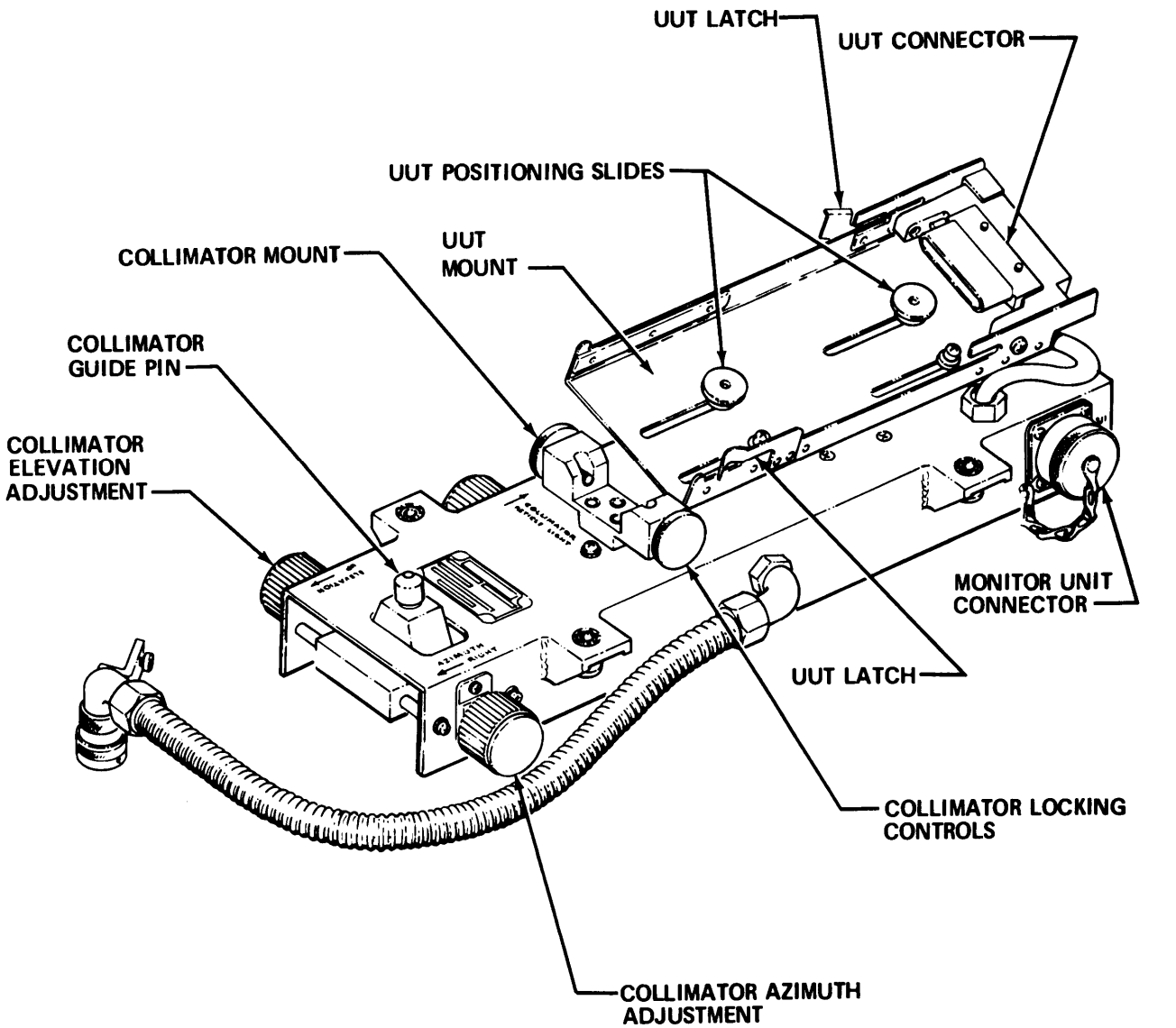


Figure 2-23. Optical alignment fixture (10277942) - mechanical functions.

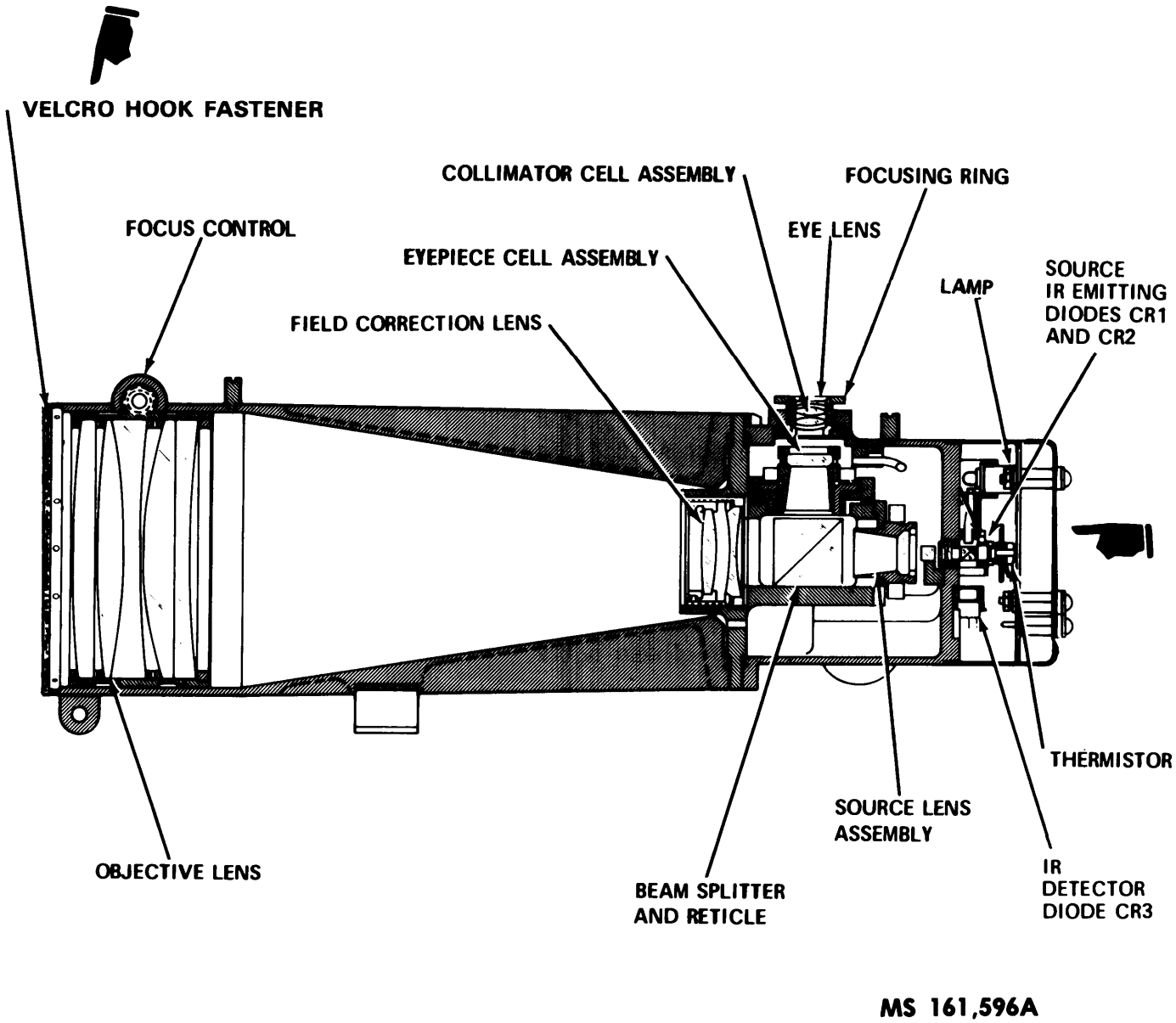


Figure 2-24 OAC - optical funtions

appears as a red dot near the center of the collimator reticle.

CAUTION

Do not touch the lens of the tetrahedral prism.

2-4. Electrical and Electronic Functions.

The following schematic diagram analysis of the electrical and electronic functions of the TTS is presented for each TTS electronic system as an aid to the technician engaged in fault isolation. Reference designations, with unit number and subassembly designations are provided in this analysis as an aid to locating circuit components during discussions.

a. TTS Monitor Unit. The TTS monitor unit contains the battery packs, battery charger power circuits, mode select switch, monitor select switch, monitor meter, testing indicators, frequency switches, thermistors, trainer trigger switch, test start/stop switch, battery charger indicators, electronic circuit cards, and associated wiring.

(1) The TTS monitor unit contains four battery packs; BT1, BT2, BT3 and BT4 (fig. 2-25, zones D1, D2 and D3). These battery packs provide primary power for the operation of the TTS and UUT. Each battery pack consists of eight series-connected, nickle cadmium “C” cell batteries.

(2) Batteries BT1 and BT2 are connected in series to form a positive (+) battery stack while BT3 and BT4 are connected together to form a negative (-) battery stack. The (+) and (-) battery stack outputs are fed to the CB1 power circuit breaker (2.0 amp trip rating).

(3) The (-) battery stack (BT3, BT4, fig. 2-25, zone D3) is connected between TTS power ground and the (-) battery distribution.

(4) The negative side of the (+) battery stack is routed through circuit card assembly 1A1, lug E1 (fig. 2-25, zone D6) to sense resistor R12 (fig. 2-26). The opposite side of the R12 sense resistor is tied to TTS power ground. The voltage drop across R12, seen at Pi-pins 6 and 12 represents the charge or discharge current through the batteries.

b. Battery Charger Circuit. The TTS battery charger circuit is contained on cards 1A11 (fig. 2-36) and 1A9 (fig. 2-34). The associated wiring in the monitor unit is shown in figure 2-25.

(1) Battery charger power system. The battery charger external power, 105-130

Vat, 50-440 Hz (115 Vac nominal), is supplied through external power connector 1J3 (fig. 2-25, zone A1) to RFI filter FL1. From filter FL, the 115 Vac is reduced to 65 Vac by step-down transformer T1. The 65 Vac output from the secondary side of T1 is coupled to card 1A11 through connector P2, pins 1 and 2 to bridge rectifier CR1, CR2, CR3, CR4 located on the electronic component assembly (fig. 2-36). The output of the bridge rectifier circuit is filtered by capacitor 1A11-C1 (fig. 2-36) (B3) producing a nominal 75 Vdc output. This voltage develops the charger current through the series pass current regulator circuit Q1, Q2, R3, R7, (fig. 2-36, zone A3), R4, R5, (fig. 2-26, zone A4) and relay K1 (fig. 2-36, zone A7) to battery charger interlock diodes CR1 and CR2 (fig. 2-36, zone B6). The charge current out of CR1 and CR2 is fed through relay K2 (fig. 2-36, zone A8), and through J1-pin 20 to the (+) side of the BT1 battery (fig. 2-25, zone D1). The current is passed through the series-connected batteries and the R12 sense resistor located on card 1A1 (fig. 2-26, zone D2) back to card 1A11 (P1) pin 21 (fig. 2-36, zone D1). The current return path is through actuated relay K2 B contacts, (fig. 2-36, zone A8) to the negative side of the CR1/CR2/CR3/CR4 bridge rectifier.

(a) Series pass current regulator - high charge rate (600 ma at ambient temperature). In this mode the regulator current path is through resistor R3 (fig. 2-36, zone A3) in parallel with resistor R4 (fig. 2-36, zone A4) (connected through the normally closed contacts of relay K1 A contacts). This combination is in series with R7, which is in parallel with R5 through the normally closed contacts of K1 B contacts. Current is then passed through CR1 and CR2 (fig. 2-36, zone B6) and out to the batteries. The AR1 (fig. 2-36, zone B6) charging current control amplifier and the Q1/Q2 current regulator maintains the voltage drop across parallel resistors R7 and R5 at approximately 6.0 Vdc when the TTS power switch is off and when the battery temperature is at 77°F (25°C). This 6.0 volt drop across 10 ohms (R7 and R5 in parallel) develops a charge current of 600 ma dc, which is the high charge rate. The AR1 output drives transistor Q1 (fig. 2-36, zone A3) which acts as a booster amplifier connected in an emitter follower arrangement to drive Q2 (fig. 2-36, zone B3). Q2 increases or decreases current to maintain a constant voltage drop across R7. The AR1 reference voltage on the non-inverting input is developed by voltage regulator VR1, VR2, Q1 (fig. 2-36, zone B4) and controlled by R7 in parallel with thermistor RT3 (fig. 2-25, zone D38), which is mounted on battery BT3. At ambient temperature (77°F) RT3 will measure 3.01K ohms. Also in parallel with R7 (fig. 2-36, zone B5) is Q1 in series with R29 on card 1A9A2 (fig.

2-34, zone B6). This path is not conducting when the TTS power switch is off. The reference then at the non-inverting input of AR1 (fig. 2-36, zone B6) will vary with temperature and when the TTS is powered. The 6.0 Vdc at AR1 pin 3 will drive Q1 until 6.0 Vdc is seen on the AR1 feedback input (AR1 inverting input, pin 2). This feedback is the voltage drop across R7 (fig. 2-36, zone B3), thus regulating the current through parallel resistors R7 and R5 (fig. 2-36, zone B3, B4).

(b) Series pass current regulator - low charge rate (300 ma at ambient temperature). In the low charge state relay K1 (fig. 2-36, zone B7) is energized which removes R4 and R5 from the parallel combination discussed previously. Now the charge path is through only R7 (fig. 2-36, zone B3) which is a 20 ohm resistor. With 6.0 Vdc drop across only R7 the battery charge current in now 300 ma.

(2) Battery charger current control system. The shift from high charge rate to low charge rate is accomplished by actuation of K1 (fig. 2-36, zone B7). The two systems which can actuate K1 are described below.

(a) Battery charger timer circuit. The timer circuit is controlled by the charge or discharge current through memory cell E1 (fig. 2-36, zone C8. This cell is an electrochemical accumulator device which plates and deplates at a rate determined by the charge or discharge rate of the batteries. The battery charge and discharge is seen as a voltage drop across battery current sensing resistor R12 on card 1A1 (fig. 2-26, zone D2) which is in series with the batteries. This voltage is fed to polarity detector AR3 and timer rate amplifier AR4 on card 1A9A1 (fig. 2-34, zone 65). The timer rate amplifier produces a current, equivalent in amplitude and polarity, to the charge or discharge rate of the batteries. This current is fed through 4.99K ohm resistor R31 (fig. 2-34, zone B5) to E1 on card 1A11 (fig. 2-36, zone C8). When the batteries are being used (being discharged), the current through E1 is reversed, which causes it to replate. In this state, E1 is a very low impedance, and the current through it develops approximately a 5 mv drop across it. When the charge is activated, a positive current is being developed by the transconductance amplifier (AR4 on card 1A9A1) and fed through E1. This current begins deplating E1 and continues until it is completely deplated. The impedance remains low until E1 is completely deplated. When deplated, the impedance avalanches to a very high value and the deplating current develops a higher voltage drop across El (>700 rev). The voltage drop across E1 is detected by timer state detector Q3 (fig. 2-36, zone D7) forward biasing it and turning it on. Q2 in turn conducts and actuates K3. When K3 is actuated, the +5 Vdc seen at J3 (zone B7) is fed

through K3, contacts AZ and A1 (zone B8), through CR5 and actuates K1 (zone B7) switching the charger to a low charge rate.

(b) Battery charger high voltage detector circuit. This circuit monitors the charger voltage across the batteries. In the case of a charger run away on excessively high charging voltage (> ±25.5 Vdc) the charger will be switched and then latched into the low charge rate. The input bridge rectifier (fig. 2-26, zone A2) is referenced to ground through each stack of batteries. The charger voltage seen across each battery stack when referenced to ground is approximately 122.5 Vdc (nominal). These voltages are seen at J1 pin 20 (+ battery) or 21 (- battery). AR2 (fig. 2-36, zone C4) inverts and amplifies the (-) battery stack voltage seen at resistor R17 by 0.324. Voltage divider R13 and R15 scales the (+) battery stack voltage by 0.327. The divider point (between R13 and R15) is summed with the diode-isolated (CR8) AR2 output and then fed to U1 through R16. If either battery stack voltage exceeds approximately 25.5 Vdc the voltage at R16 will exceed 8.2 Vdc and U1 output will switch high (U1 pin 1 is referenced at 8.2 Vdc by VR6 and R19, fig. 2-36, zone C5. The relay driver actuates K1, placing the unit to low charge. When K1 actuates, the (+) battery stack charge voltage is fed through K1 contacts A2 and A1, through R12 to U1 pin 10 to lock U1 in the high state. K1 will remain energized until a reset is given, which is discussed in the following paragraph.

(3) Battery charger reset system. The TTS test reset which occurs at test start/stop switch actuation is a low logic level (<0.5 Vdc) which lasts for 1.9 seconds. This signal is fed into card 1A11 through pin 12 to logic U3A and U3C. At this time U2 pin 3 goes low, dropping out K1 and returning the battery charger back to high charge. At the same time, Q3 (fig. 2-36, zone D7) base goes to 0 Vdc, switching Q3 and Q2 off and dropping out K3, allowing E1 to be discharged.

(4) Battery charger, charing current override circuit. This circuit, which is located on card 1A9 (fig. 2-34, zone B6, B7), increases battery charging current when the test start/stop switch actuates primary power interlock K1 on the 1A1 card (fig. 2-26, zone C3). Battery voltage (+) is applied from card 1A1 pin 15 (fig. 2-25, zone D7) through card 1A9 pin 16 (fig. 2-25, zone D35), through R33 to the base of Q2 on card 1A9A2 (fig. 2-34, zone B7) forward biasing it and turning it on. Q2 conducting turns Q1 on allowing current to flow through it. The Q1, R29 series combination is in parallel with resistor R7 in the battery charger charging current control amplifier circuit (fig. 2-36, zone B5) on card 1A11. This parallel current path reduces the total impedance and allows more current to flow, which increases

the voltage at J8 (fig. 2-36, zone B5) and increasing current through the series-pass regulator, increasing battery charge current through the batteries to approximately 650 ma.

(5) Battery charger, timer charge rate amplifier. The timer charge rate amplifier, consisting of AR4 and its associated circuitry (fig. 2-34, zone B4, B5) produces a charge or discharge current to E1 (fig. 2-36, zone C8) equivalent to the current flow through the batteries. The battery charge or discharge is seen as a voltage drop across battery current sensing resistor R12 on card 1A1 (fig. 2-26, zone D2). The voltage is fed from card 1A1 pins 6 and 12 (fig. 2-25, zone D7) to card 1A9 pins 39 and 41 (fig. 2-25, zone D35). At ambient temperature (77°F) with the TTS power switch off and the battery charger charging light on (charging at high rate), 600 ma will be flowing through sense resistor R12, developing 120 mVdc between pins 39(+) and 41(-) on the 1A9 card (fig. 2-34, zone C2). This +120 mVdc signal is seen at voltage comparator AR3 pin 2 and compared against a reference voltage of approximately +12 mVdc (from voltage divider R32 and R33). The AR3 output will be at negative saturation which will pinch off FET switch Q5 (zone B4) and prevent its conduction. With Q5 pinched off, scaling resistor R30 is in the circuit. The +120 mVdc seen at pin 39 develops a current flow through R27, R29, R30, R31, K4 B, pin 36, pin 25 on card 1A11 to E1 (fig. 2-36, zone C8) setting up voltage drops across each component. The voltage drop seen between R30 and R31 (fig. 2-34, zones B4, B5) is amplified by AR4 and fed back through the divider chain, minus resistor R27. This regulates the current flow through the divider chain including E1. This positive current through E1 causes it to deplate. When the battery charger is off and current is being drained from the batteries, a negative voltage will be seen at AR3 pin 2 causing the output to go to plus saturation and allowing FET switch Q5 to conduct, which shorts out resistor R30. This changes the scaling of the divider. With a negative voltage at pin 39 the current will flow through El in the opposite direction causing it to plate.

(6) Timer supply voltage generator. The + and - 15 Vdc required to power the battery charger controls (card 1A11) and the timer charge rate amplifier circuit (card 1A9) may be provided from either of two sources.

(a) Charger power supply voltage. When TTS main power is off and the battery and the battery charger is on, the +15 Vdc is developed by VR1 and Q3 on card 1A11 (fig. 2-36, zone B3) which is powered from the series-pass regulator (approximately +29 Vdc nominal). The -15 Vdc is developed by VR5 which is powered from

charger supply voltage (low) (approximately -22.5 Vdc nominal).

(b) Battery power timer supply voltage. When the battery charger is off and test power is being taken from the TTS batteries, the timer supply voltage comes from the + and - CB1 output (fig. 2-25, zone D4) through card 1A9 pins 28 and 32 (fig. 2-25, zone D36), through the K3 contacts (fig. 2-34, zone B3) to dropping resistors R20 and R23. The R20 and R23 output is nominally + and - 17 Vdc but can swing as much as 15 to 21 Vdc. K3 is energized when a test start sequence is initiated or when the OAC test lights are illuminated. When the test start/stop switch is actuated and K1 (card 1A1, fig. 2-26, zone C3) is energized, the charging current override circuit (fig. 2-34, zones B6, B7) produces a ground (<0.5 Vdc) at the Q2 collector which forward biases Q2 (zone B2) turning it on and actuating K3. The second method of actuating K3 is by turning on one of the OAC lamps. When one of the OAF light switches are turned on, -20.0 Vdc is fed from card 2A1 (fig. 2-38) pin 4 through the OAF to J1 pin i (fig. 2-37, zone B4), through the TTS test cable to monitor unit J1-i (fig. 2-25, zone C39), through card 1A9 pin 26 (fig. 2-25, zone D39) to R19 and the base of Q2 on card 1A9 (fig. 2-349 zone B2). This -20 Vdc turns on Q2 and actuates K3. The OAF lamp circuit will be discussed in a later paragraph.

(7) Battery charger timer synchronization circuit. This circuit synchronizes E1 (fig. 2-36, zone C8) with the charge state of the batteries. If new batteries (fully charged) are installed, it is necessary to place the battery charger memory cell (E1) in its fully deplated state (E1 impedance has avalanched to its high state). This is accomplished by applying +28 Vdc (nominal) through J1 pin y, card 1A9 pin 38 (fig. 2-25, zone D39), through the normally closed contacts of K4 (fig. 2-34, zone D4) to the gate of SCR Q3. This positive voltage turns on SCR (Q3) and actuates K4. The current path through R24 keeps the K4 energized. With K4 energized, the current path from pin 38, is through R25, through actuated K4, through monitor unit wiring to 1A11 pin 25 (fig. 2-25, zone A7) and E1. This current deplates E1 until it develops a high impedance. This high impedance develops approximately 700 mVdc across it, which forward biases Q4 on 1A9A1 (fig. 2-34, zone D4) and causes it to conduct. When Q4 conducts, it shorts out the K4 coil, causing it to reenergize and remove power from E1, SCR Q3 and Q4 will not reset until power has been removed from pin 38.

(8) Battery charing lamp indicator. When the battery charger CB is turned on, the charging lamp will illuminate until K3 on card 1A11A1 (fig. 2-36, zone B8) is

actuated. At this time +5 Vdc (on K3, contact A2) is passed through the K3 normally open contacts, through J1 pin 23 to full charge lamp DS4 (fig. 2-25, zone D46). The low side of DS4 returns through card 1A11 pin 16 to the charger rectifier low which is -22.5 Vdc nominal (referenced to ground).

c. TTS Power Control System. Cards 1A1 (fig. 2-26), 1A2 (fig. 2-27), 1A3 (fig. 2-28), 1A6 (fig. 2-31), and 1A7 (fig. 2-32) contain the TTS power control system. The associated wiring in the monitor unit is shown on fig. 2-25. The power control system is broken down into the following categories:

(1) Power application circuit (test start). The test start circuit which is necessary to initiate TTS testing is controlled on the 1A1 card. In the monitor unit, battery power is fed through CB1 to lugs E3 and E4 on the 1A1 card. This battery voltage arms K1 latch coil (X1) and both K1 wipers (fig. 2-26, zones C3 and B3). The test start/stop switch S3 (fig. 2-25, zone D45) is armed by mode switch S6 whenever it is in the trigger output, boresight, missile command, trainer, or self test positions. When the TTS test start/stop switch S3 is depressed, a ground is supplied through J1-3 and actuates 1A1 K1 latch coil (X1, X2) causing the contacts to switch to their normally open positions. At this time + battery voltage from lugs E3 is fed through the L1 filter choke and out J1-11. Battery voltage from lug E4 is fed through choke L2 to J1-13. The primary power relay K1 is a mechanical latch device. K1 is actuated by the latch coil (X1 and X2) and reset by the reset coil (Y1 and Y2). The voltage seen at pins 11 and 13 is fed to the + and - 13 Vdc regulators on card 1A2. The actuated contacts of K1 on 1A1 also apply + and - battery voltage to the +5 Vdc digital power supply (PS1, lugs 10 and 12) turning it on. When K1 is actuated, the + battery voltage arms the K1 reset coil by applying + battery voltage to reset coil terminal Y1. Power is then applied to the TTS.

(2) Test stop. The TTS test may be stopped in either of two ways; by activation of the test start/stop switch (after Ts +4 sec.) or by allowing the master counter to activate the stop circuit.

(a) When the test start/stop switch is depressed, a ground is supplied to 1A3 (fig. 2-28) pin 37. This ground results in a +5 Vdc positive pulse at the collector of Q1. This output is delayed by U1B and fed as a positive pulse to U2A (U1B does not invert the output). At approximately 6 seconds after the test start/stop switch has been actuated, a positive-going step from 1A4 will be seen at pin 25 arming the U2A gate. If the testing lamps are on, the test stop gate will be

high (seen at P1-23) which arms U1A. With U2A and U1A armed, the positive pulse seen at U1B output will be fed through U2A and U1A forward biasing Q2 and causing the output at P1-33 to go low. This is seen as a low on 1A1 pin 4 (fig. 2-26). This low energizes K1 reset coil (Y1 and Y2) and resets K1 to the power off state.

(b) The second test stop method is automatic and occurs when the test sequence is complete and 1A4 pin 25 goes low (fig. 2-29). This pulse is fed through 1A3 pin 23 to U1A (fig. 2-28) driving the output high, forward biasing Q2, and driving the output low.

(3) Test reset. The reset generator on card 1A3 (fig. 2-28) which consists of Q3, Q4, Q5, and VR1 and VR2 (fig. 2-28, zones B2 and B3) comprises a 1.9 second one-shot multivibrator. In the quiescent state, + battery voltage is seen at pin 29. No voltage is present on pin 40 (test reset generator trigger pulse), on pin 1 (+5 Vdc digital) and Q3, Q4 and Q5 are biased off. Normally the voltage at pin 38 would be high (> 2.5 Vdc) but at this time the +5 Vdc digital power supply has not been turned on. When the test start/stop switch is actuated, K1 on card 1A1 (fig. 2-26) is energized and the + battery voltage is fed through 1A1 J1-15 to 1A3 pin 40 (fig. 2-28). Simultaneously, the +5 Vdc digital power supply is turned on and +5 Vdc is supplied to pin 1. This results in the collector of Q5, going high. The + battery voltage positive step, seen at pin 40, instantaneously passes current through C6, CR2, R11 and R12, developing a positive voltage drop across R12, which turns on Q3. This turns on Q4 and Q5 and feeds back a current which charges C3 through R8, and R12 in parallel with R13 to power ground. Since Q3 is forward biased by the voltage drop across R12 it will remain on until the charge current through C3 decreases enough for the voltage drop across R12 to turn Q3 off which will also turn Q5 off. This results in the output of Q5 (collector) being low for 1.9 seconds. VR2 (6.2V zener diode) acts as an overvoltage protection device.

(4) +13 Vdc prime power. Since the plus and minus 13 Vdc series regulators are nearly identical, the plus regulator will be described in detail and the minus regulator will be only briefly discussed. Card 1A2 (fig. 2-27) contains the 13 volt power regulators, open voltage protective crowbar circuits and the power interlock circuitry. When K1 (fig. 2-26, zone A3, C3) is actuated, + and - battery voltage is fed to the 1A2 regulators through pins 8(+) and 7(-) (fig. 2-25, zone A1O). The +13 Vdc series regulator may be divided into several sections:

(a) Preregulator. This is a current regulator whose output is developed across a voltage divider consisting of R26, R8, R9, R10 and R12 (fig. 2-27, zone

A3) in series with Q1 with the actual output being approximately 13.5 Vdc between R26 and R8. The object of this regulator is to maintain a constant current through Q1 and the voltage divider. This is done by taking the voltage on the wiper of R10 and comparing it with the VR2 regulator voltage (6.2 Vdc). If the final regulator output (at P1-17) is +13.0 Vdc the R10 wiper will be approximately 6.2 Vdc and the AR1 output will be zero volts. If the R10 wiper voltage is not 6.2 Vdc, the AR1 output will bias Q3 which in turn will bias Q1 to increase or decrease the current through the voltage divider, increasing or decreasing the output voltage seen between R26 and R8. When the R10 wiper reaches 6.2 Vdc the AR1 output will return to zero.

(b) Final regulator. The output of the preregulator, drives the base of final regulator power transistor Q1 on 1A2A2 (fig. 2-27, zone A7). The 1A2A2 Q1 emitter, which is the +13 Vdc power output, feeds this voltage out P1-7 (zone B2).

(c) Current limit control. The current control is performed by R4, Q2 and Q4 (fig. 2-27, zone A4, A3). As the current through R4 and final regulator Q1 (fig. 2-27, zone A7) becomes larger, the voltage drop across R4 will become larger. When the +13 Vdc current becomes excessive the voltage drop across R4 will forward bias Q2. Q2 conducting initially draws collector current through R27, forward biasing Q4 and causing it to conduct. Q4 conducting shorts the output of AR1 to ground, which in turn cuts off Q3 and Q1 and drops the voltage between R26 and R8 to zero.

(5) -13 Vdc prime power. The operation of this regulator is nearly identical to the +13 Vdc regulator, therefore, only a brief description is given here. In this circuit, the current regulator output is developed across voltage divider R19, R22, and R25 in series with Q5 and VR5 (fig. 2-27, zone B3, C3) with the actual output being approximately -19.5 Vdc between R19 and R22. This output of the preregulator biases the base of final regulator power transistor Q2 on 1A2A2 (zone C7). This base biases produces -13 Vdc at the Q2 collector which is the -13 Vdc bus and is fed out P1-2 (zone C2). Voltage divider R14, R16, and R20 (zone B4) produces the regulator feedback from the wiper of R16 to regulator differential amplifier AR2. This regulator and the current limit control functions the same as was described for the +13 Vdc prime power circuit.

(6) +5 Vdc digital power. Card 1A1 plus battery and minus battery K1 relay contact outputs (fig. 2-26, zone B3, C3) are supplied to a PS1 DC to AC inverter (fig. 2-26, zone A4) and then rectified by full wave rectifier CR2/CR3. This output powers the +5 Vdc digital power supply which is a switching regulator device

with current limiting. The DC to AC converter circuit isolates the +5 Vdc digital bus feedback noise and maintains a higher output voltage during normal operation. The power supply load current path is through Q2, L3, R10, L4 and out to the TTS bus load.

(a) AR1 is a switching regulator device whose output at terminal 2 is a pulse waveform with a given duty cycle which is between 20kHz and 100kHz depending on the power supply load and the voltage drop across divider chain R15, R16, and R17. This pulse waveform out of AR1 drives series-pass transistors Q1 and Q2 off and on. This pulse waveform is filtered to a direct current by L3, L4, C7 and C8. The output voltage of the filters will be the average peak voltage value of the pulse waveform. The frequency of the AR1 pulse output is controlled by the feedback circuit from the R16 potentiometer wiper, in the R15, R16, R17 voltage divider. The RJ6 wiper is adjusted for a duty cycle, which after being filtered by L3, L4, C7, and C8, will give a voltage output of +5.O Vdc. CR7 acts as a catch diode, providing a continuous path for the inductor current when Q1 and Q2 turn off. R13 provides positive feedback to the AR1 switching regulator. C6 is a feedback component to minimize output ripple.

(b) Current limiting of the +5 Vdc power supply. The peak current through the switching transistor Q1 is sensed by R10. When the voltage drop across R10 becomes large enough to forward bias Q4, it will conduct and turn on Q3 which produces a higher voltage (or more current) to AR1 feedback terminal 6. This produces a slower duty cycle and reduces the L4 output voltage.

(7) 5 Vdc reference power. The plus and minus 5 Vdc reference regulators located on 1A6 (fig. 2-31, zone A3 thru A7) are basic regulator circuits consisting of differential amplifiers and transistor drivers. This circuit is powered by plus and minus 13 Vdc from 1A2 pins 38 and 40.

(a) The +5 Vdc regulated output at the Q1 emitter (fig. 2-31, zone 5) is developed across voltage divider R2, Q1, and R13. The AR1 noninverted input is biased by +5 Vdc from voltage divider regulator circuit R1, VR1, R7, R8, and R11. This voltage is compared with the negative feedback voltage across R13. The AR1 output will increase or decrease the current through Q1 until the voltage drop across R13 equals the reference voltage at the wiper arm of R8.

(b) The -5 Vdc regulator consists of inverting amplifier AR2 and Q2 with variable gain. Q2 provides the power to the output. The feedback voltage from across R5 maintains the -5 Vdc output.

(8) Crowbar protection circuit. Crowbars U1, U2, and U3 on 1A2 (fig. 2-27, zones A5, B5) are overvoltage protection devices used to sense an overvoltage condition on the +13 Vdc bus (P1-17, zone B2), the -13 Vdc bus (P1-2, zone C2), and the +5 Vdc digital bus (P1-1O, zone A2). When an overvoltage is sensed on the crowbar circuit input, the output will switch to digital LO (<0.5 Vdc). The U1 and U2 crowbar outputs (marked 5W) are tied together and are fed out P1-3, (zone A2) through 1A1 pin 4, to the reset coil (Y2) of K1. When the U1 or U2 crowbar detects an overvoltage its output goes L0 which actuates K1 reset coil on 1A1 removing all TTS power. The U1 crowbar actuates at +6.25 Vdc, the U2 crowbar actuates at +15.5 Vdc and U3 actuates at -15.5 Vdc. Each crowbar has a self test point which, when biased, will simulate an overvoltage in the crowbar. These inputs are made at P1-4, P1-5 and P1-6. The output actuate portion of U3 is slightly different from U1 and U2. The LO output from U3 will forward bias transistor Q1 (zones A6), applying +13 Vdc to the self test point of U2 which drives its output LO.

(9) Power ground/system ground tie. The TTS single point ground (when the signal ground, power ground and chassis ground are all tied together) is in the UUT when it is connected. These grounds must be tied together for the TTS analog systems to function. In the trainer mode, when the UUT is not connected to the OAF, the ground tie is made by K1 on 1A6 (fig. 2-31, zone B6). K1 is actuated by -13 Vdc from lug 15 (trainer position) of mode switch S6-C (fig. 2-25, zone B3). The S6-C wiper is connected to -13 Vdc at P1-38 on 1A2.

(10) Power distribution. The + and - 13 Vdc power is distributed to the systems via seven power relays. Five of these relays are located on 1A2 (fig. 2-27), one is located on 1A7 (fig. 2-32), and one is located on 1A3 (fig. 2-28). The + and - 13 Vdc test power, which operates all TTS analog circuits, is armed by, K1 (fig. 2-27, zone C3). The + and - 13 Vdc power from the output of the + and - 13 Vdc regulators is fed through the normally closed contacts of K1 (zone C3), K3 (zone C4), K1 (1A3A2, fig. 2-28, zone A6) and K1 (1A7A2, fig. 2-32, zone C6). At 21 seconds after test reset, in any mode except self test, the test power gate signal at P1-33 (fig. 2-27, zone C2) will go HI, driving U1 output HI and actuating K1. In any mode except self test P1-32 (zone C2) will be open or logic HI. At this time all test power is removed. In the self test mode, P1-32 will be LO keeping K1 deenergized. The remaining power control relays are controlled by the diode matrix CR5, CR7, CR8, CR9, CR1O, CR11, CR12, (fig. 2-27, zone D2, D3 and D4) and mode select switch S6 pole C (fig. 2-25, zone B3) refer to the block diagram (fig. 2-5).

(11) Self test load. In the self test mode, -13 Vdc is fed through diode matrix actuating K1 on the 1A2A2A1 card (fig. 2-27, zone B6), connecting load resistor R1 across the +13 Vdc bus and connecting R2 across the -13 Vdc bus. This simulates a UUT load current during a self test operation.

d. OAC Testing Lamps. The OAC lamps are used to set up and align the OAC with the UUT. This alignment is performed after the power circuit breaker has been turned on and prior to actuation of the test start/stop switch for a test sequence. Each light is individually controlled by a switch and an intensity-control potentiometer on the OAF. The tracker reticle light (DS3) (fig. 2-37, zone D7) is mounted external to the UUT eyepiece while its associated test cable is connected to OAF connector J2 (fig. 2-37, zone D6). The self test light (DS1) and the reticle light (DS2) (fig. 2-39, zone D2) are mounted in the OAC. When the monitor unit power circuit breaker (CB1) (fig. 2-25, zone D5) is turned on, plus and minus battery power is fed through the normally closed contacts of 1A1 K1, (fig. 2-26, zone B3 and C3) and out J1-1 and J1-2 (zone B2 and C2). This voltage is fed out monitor unit J1 (pins j and k, fig. 2-25, zone C7), through the TTS test cable and through OAF J1, pins j and k (fig. 2-37, zone 65) to 2Al J4 pins 5 and 6. On 2A1 (fig. 2-38, zone D1) plus battery power at P1-5, is applied to the collector of Q8. The self test lamp, the collimator reticle lamp, or the tracker reticle lamp require approximately 31 Vdc for full illumination (the tracker reticle lamp circuit contains a 200 ohm resistor). VR2, VR3, and Q8 comprise a simple +31 Vdc regulator circuit whose output at Q8 emitter powers the three lamps through three control potentiometers and three switches. Plus battery voltage feeds the collector of Q8. VR2 and VR3 provide a Q8 base bias of +31 Vdc, referenced to the plus battery input at 2A1 pin 6, which regulates Q8 emitter voltage to approximately +31 Vdc, referenced to the minus battery input. This +31.0 Vdc is fed out 2A1 pin 7 to the self test, collimator reticle, and tracker reticle lamps.

e. Monitor Select System. The monitor circuitry makes available the panel readout of all major TTS voltages. Refer to block diagram figure 2-19. Each voltage parameter is selected by TTS monitor select switch S2 (fig. 2-25, zone C1, C2, C3, and C4). The monitor select switch is a ten-position four-pole rotary switch, and selects voltage parameters to be read on the monitor meter circuit which consists of a 1 ma full scale ammeter (M1) (fig. 2-25, zone B5) in parallel with approximately 701 ohms and in series with approximately 13.8 Kohms of resistance (the 13.8 Kohms series resistance is not used for battery voltage readouts). The

monitor select switch permits readouts of the following parameters:

(1) Power regulators. Monitor select switch pole C and D wipers (fig. 2-25, zone C3 and C4), when in the +13 Vdc, -13 Vdc, +5 Vdc + REF, or - REF position, applies these regulator output voltages through P1-35 on 1A3 (fig. 2-25, zone D10) to the series-scaling resistors R30 and R31 on 1A3 (fig. 2-28, zone A4). The output at P1-26 is applied directly to the plus side of the monitor meter (M1) (fig. 2-25, zone C5). The meter negative return is through the S2-D wiper to the regulator return. R32 and R33 are in parallel with the meter on 1A3 (fig. 2-28, zone A4).

(2) IR output. When the TTS monitor select switch is in the IR output position, monitor meter indicates the OAC IR diode radiated output level. The OAC radiating diode, CR1 or CR2 (fig. 2-39, zone C2), signal is monitored by OAC detector diode CR3 (fig. 2-39, zone B2). This signal is amplified by AR1 on 3A1 (fig. 2-39), rectified by the AR5 circuit on 1A9A2 (fig. 2-34, zone A6), summed with IR source dc voltage by AR6 on 1A9A2 and then applied to the monitor meter through monitor select switch (S2).

(a) OAC IR detector amplifier. Photo detector diode CR3 (fig. 2-39, zone 62) is initially current-biased by applying +13 Vdc through scaling resistors R1 and R3, through detector diode CR3 to power ground. This provides a continuous current through the detector diode to establish a current operating level for the input signal. When the TTS is in the boresight mode, at 5 seconds elapsed time, the near-center IR source diode (CR1) (fig. 2-39, zone C2) will be radiating at a nominal IR intensity. The IR output from CR1 bombards photo detector diode CR3 and causes approximately 257 uamps of modulated signal to flow through it. This current produces approximately a 3.2 mv RMS signal (sine wave) across photodetector diode CR3, which is fed through isolation capacitor C4 (fig. 2-39, zone B3) to AR1. C4 removes the DC bias and only allows the AC signal to be applied to the input of AR1. AR1 is a noninverting amplifier with a nominal gain of 78. The output is developed across R10 and fed out pin A of 3A1. When the IR source diodes CR1 or CR2 are radiating at high intensity, it is necessary for CR3 detector diode to be current-biased at a higher level. At this time the IR monitor gain select gate goes HI energizing K1 (fig. 2-39, zone A3), reducing bias resistance by paralleling R4 with R3 and increasing CR3 current. This scales the CR3 diode signal to approximately the same voltage level seen at low intensity IR radiation. Capacitor C2 feeds back high frequency noise. Output at pin A 3A1 is fed through the OAF, the TTS cables and the monitor unit to 1A9, pin 19 (fig. 2-25, zone D37).

(b) IR monitor half-wave rectifier. With the TTS in boresight mode and the time stopped at approximately 5.0 seconds, the IR radiating diode will be at a low intensity level and the AC sine wave at JA9 pin 19 (fig. 2-34, zone B2) will be 250 mv RMS. This sine wave is halfwave rectified by AR5 and fed to the summing circuit (zone A7). CR1 allows only a negative feedback to the input of AR1. Scaling resistors R19 and R24 (zone A6 and A7) give an amplifier gain of -20. The output at CR2 (zone A7) anode is a 7.07 volt peak pulsating signal. When reading at this point with a DC meter, the meter will read the peak voltage divided by π which is 2.25 Vdc. This signal is fed to AR6 filter and summing amplifier (zone A7).

(c) Filter and summing amplifier. AR6 sums the IR monitor output, from AR5 (fig. 2-34, zone A7), with a nominal 5.0 Vdc (at ambient temperature) reference voltage from 1A8 pin 40 (fig. 2-33). This voltage is temperature-compensated by a 1 Kohm thermistor in the OAC. AR6 (fig. 2-34, zone A7), reference voltage gain is approximately 0.412 and is determined by R21, R22 and R23. The IR monitor gain is approximately 2.43 and is determined by R26, R22 and R23. These two amplified voltages are added, and the AR6 output (zone A8) becomes -7.52 Vdc. This output is fed out 1A9 pin 4 (fig. 2-25, zone D36) to the monitor select S2-D, lug 6 (fig. 2-25, zone C4). This -7.5 Vdc output will deflect the monitor meter to mid-scale.

(3) Battery monitor. Each battery pack can be read by differential amplifier AR1 on 1A9A1 (fig. 2-34, zone A4). The input to AR1 is applied through the energized contacts of K1 on card 1A9A1 (zone A3) and through the energized contacts of K2 to monitor meter (positive lug, fig. 2-25, zone B5) in parallel with R32, R33 on 1A3A1 (fig. 2-28, zone A4). The meter negative lug (fig. 2-25, zone C5) is fed through monitor select switch (S2) (zone C4) to battery monitor reference voltage generator AR2 on 1A9A1 (fig. 2-34, zone C3). AR2 is a thermistor-controlled bucking voltage generator which biases the monitor meter. This circuit is used to maintain a constant system scaling at temperature extremes.

(a) Wiring and switching. Monitor select switch (S2) poles A and B are used to monitor the voltage drop across each of the TTS battery packs (reference fig. 2-19 and 2-25, zones C1 and C2). When the monitor select switch is in one of the battery monitor positions, the voltage is fed through the S2-A and S2-B wipers to the battery stack differential amplifier on 1A9 P1-33 and 34 (fig. 2-34, zone A2 and fig. 2-25, zone D36). The differential amplifier output voltage from 1A9, pin 30 (fig. 2-25, zone D36) is then routed to the positive side of the monitor meter (fig. 2-25, zone B5). The monitor meter reference voltage generator output on pin

23 (fig. 2-25, zone D36) is fed through contacts 7, 8, 9, 10 and wiper of S2-D to the negative side of the monitor meter (fig. 2-25, zone C5).

(b) Battery stack differential amplifier. Battery stack differential amplifier, AR1 on 1A9A1 (fig. 2-34, zone A4), is armed by K1, which actuates when + and - 13 Vdc power is applied. The AR1 output, scaled down by R9, VR1, and R1O, forward-biases Q1 when AR1 output is greater than 1.5 Vdc, this actuates K2. The actuated K2 applies the AR1 output through P1-30 to the monitor meter positive terminal (fig. 2-25, zone C5).

(c) Battery monitor reference voltage generator circuit (bucking voltage generator). AR2 on 1A9A1 (fig. 2-34, zone C3) is basically a voltage amplifier. The -6.2 Vdc developed across VR2 is amplified by AR2 to 8.62 Vdc at ambient temperature (77°F). The gain of AR2 is determined by R13, R14, R15, R11, R12 (zone C3) and thermistor RT1 (fig. 2-25, zone D38). The gain will vary with temperature and adjustment of R12. The output is fed through scaling components R17, R18 and RT2 (fig. 2-25, zone D38) and fed out pin 23 (fig. 2-34, zone C2).

f. Timing System. The timing and master counter system circuits are primarily contained on 1A4 (fig. 2-29) with support circuitry on 1A8 (fig. 2-33), 1A9 (fig. 2-34), and 1A10 (fig. 2-35). The associated wiring in the monitor unit is shown in figure 2-25.

(1) Crystal controlled digital clock. The clock circuit for the master counter is located on 1A4A2 (fig. 2-29). AR1 (voltage comparator and Y1 (fig. 2-29, zone B7, B8) comprise a crystal controlled oscillator whose output is shaped by symmetry flip-flop U15. The oscillator output is a 20 kHz 5 V peak symmetrical square wave with a pulse width of 50 usec. Positive feedback is provided from the AR1 output via the series resonant impedance of crystal oscillator (Y1) (fig. 2-29, zone B7) to the noninverting input of AR1. The DC operating point is biased by R1, R2, and VR1. The negative feedback noise and overshoot is removed by C2. Symmetry flip-flop U15 (fig. 2-29, zone B7) is a divide-by-two logic, which switches on the negative-going pulse of the AR1 output. The U15 output is a symmetrical 10 kHz square wave. The clock pulse out of U15 may be inhibited by placing a ground on pin 5 and is monitored at J1-x (fig. 2-25, zone C23) on he TTS monitor panel.

(2) Master counter. The U15 output (fig. 2-29, zone B7) is fed to the BCD (binary coded decimal) decade counters, consisting of U1, U2, U3, and U4 on 1A4A2 (fig. 2-29, zone A6, A7, A8) and U1 and U2 on 1A4A1 (fig. 2-29, zone A2, A3). U1 through (zone A6, A7, A8) U4 and U1 and U2 (zone A2, A3) are high speed BCD fully

synchronous decade counters which are cascaded to provide multistage synchronous counting.

(a) Each BCD decade counter is a divide-by-two counter with each output being the result of a binary division, (the input clock pulse will be divided by 1, 2, 4, and 8). The final output at pin 15 will go HI on the 9th clock pulse and will return LO on the 10th pulse. The 1, 2, 4, 8 binary outputs are seen on pins 14, 13, 12, 11 and the final output (tenth count) is seen on pin 15 of the module. As an example, the frequency output at pin 11 of BCD U1 (assuming the 10 kHz clock input at pin 2) will be 10,000 divided by 8 or 1250 Hz. Converting this to PRT would be 1 divided by 1250 or 0.8 msec. The U1 output at pins 12, 13, and 14 would be 2500 Hz (.4 msec.), 5000 Hz (.2 msec.) and 10,000 Hz (.1 msec.) respectively. Pin 15 will go HI at O.9 msec and LO at 1.0 msec (1000 Hz).

(b) Each BCD decade counter has the clock input at pin 2 and the terminal count output at pin 15. The terminal count output (TC) goes HI when the counter output is equivalent to a decimal 9 (goes HI after the 9th clock pulse). After the 10th clock pulse the counter returns to zero. Pins (7) and (10) on each BCD decade counter (except U1 and U2) are a count enable input (CE). The individual module will not begin to count until the two CE inputs are HI.

(c) Counter U1 (fig. 2-29, zone A8) is initially enabled when +5 Vdc is applied to pin 16. Since pins 7 and 10 are not connected on U1 (the equivalent input on these pins will be a HI) this counter is continuously enabled and counts as long as clock pulses are present and the reset at pin 1 is HI.

(d) The test sequence starts when the test reset ground is removed from pin 1 of each counter module (U1 through U4 on 1A4A2 and U1 and U2 on card 1A4A1). This constitutes Ts.

(e) The test reset to the counters is generated on 1A3 and fed to 1A4A1 P1-17 (fig. 2-29, zone B1). When reset is applied, all count inputs are inhibited and all outputs are returned to logic zero. At this time U1 begins to count the clock input at pin 2. The pin 11 output is a LO going HI digital output which occurs 0.8 msec [1 ÷ (10,000 Hz +8)] after reset pin 1. U1 output at pin 15 goes HI at the end of the 9th count of the input clock to pin 2 and remains HI for one count. This HI arms the U2 counter (pin 7, zone A7) and allows the U2 count to begin with the next negative going pulse of the clock input (U2, pin 2). This HI from U1 pin 15 also arms the remaining counters (U3, U4 on 1A4A2 and U1, U2 on 1A4A1), however, these remaining counters will not count down because they are held off (LO) by pin

15 on the preceding counters (U2, U3, U4 on 1A4A2 and U1 on 1A4A1) (Pin 15 will remain LO until the 9th count of the clock).

(f) Since the counter modules are connected in cascade (each is armed by the previous counter) the next stage advances by one count for every 10 counts of the preceding stage. This results in U2 being a divide by 20 device, U3 being a divide by 200 device and so on through the counter chain.

(g) The U2 pin 14 output will be a 10,000 HZ ÷ 10 or 1000 Hz (PRT= 1 ÷ 1000 = 1.0 msec) output. Pin 11 will be a 10,000 Hz ÷ 80 or 125Hz (PRT=1 ÷ 125 = 8.0 msec). At 9.0 msec U2 pin 15 will go HI and arm U3 pin 10 allowing U3 to count (U3 pin 7 has already been enabled). The outputs from U3 will be as shown on the schematic (fig. 2-29). The remaining counters perform the same as counters U2 and U3 on 1A4A2 (zone A7, A8). The counter outputs available are as shown on the 1A4 schematic (fig. 2-29).

(3) Time sequence decodes. The master counter outputs are used to develop TTS testing gates and envelopes. Since these are basic logic structures only a few will be discussed.

(a) First motion discrete gate. This pulse is generated on 1A4A2 (fig. 2-29, zone B14) with its output at P1-3 (zone D9). U8A and U8B (zone B14) are connected to forma RS (reset, set) circuit or memory holder. During the reset period pin 5 of U8B is held LO which holds the output HI. With a HI at U8A, pins 1 and 2 will drive the U8A output LO. This LO is fed back to U8B pin 4 to hold its output HI. At this time the U8A/U8B RS circuit is held in the reset position. U9B (zone B14) is fed by three counter outputs, .2 seconds, .04 seconds and .01 seconds. At Ts each of the counter outputs will be LO and will remain LO until all three counter input gates have gone HI (at Ts + 250 msec) at which time the U9B inputs will be in coincidence and the U9B output will switch LO. This LO into the U8A/U8B RS circuit will drive U8A output HI, which drives the U8B output LO (the test reset at U8B pin 5 is HI after the reset). At this time the information at the U8B output is latched up and will not respond to any change on U8A pin 1. The output of this circuit at U8B is a HI level going LO at Ts +250 msec.

(b) Test stop gate. This circuit is located on 1A4A1 (fig. 2-29, zone D2 and D3) with its output at P1-25.

1. When the TTS mode switch (S6) is in any mode except trainer, the input at 1A4A1 P1-32 (zone D1) and U6B pin 4 (fig. 2-29, zone D2) will be HI. The composite input at P1-31 (zone D1), will be LO if all systems are go and is fed to U6B pin 5 (zone D2).

2. In any mode except trigger output when the composite input is LO, the U6B output will go HI which will arm U5B with a HI. At 10 seconds after reset, pin 13 of U5B will go HI and at 20 seconds after reset, pin 12 will go HI. So at Ts +30 seconds the U5B output will switch LO driving U6D output HI. Since U6C pin 9 is an external test input, it will be HI and U6C output will switch LO. This LO is fed out P1-25 (fig. 2-29, zone D1) and will reset K1 on card 1A1 (fig. 2-26, zone A2).

3. When the composite input at P1-31 (fig. 2-29, zone D1) is HI (composite no-go) the U6B output will go LO driving U5B output HI, which arms U6D. When the 20 second input at U6A pin 1 goes HI and the 40 second input goes HI (which will be at 60 seconds), the U6A output will go LO driving U6D output HI and U6C output LO.

4. When the TTS mode switch (S6) is in the trainer position, a ground (LO) is seen at P1-32 (fig. 2-29, zone D1) which arms the 30 second summing gate U5B and the U6C output will go LO after 30 seconds.

(c) IR source intensity logic. This circuit is located on 1A8A1, (fig. 2-33, zone A1, A2, A3), with its output at pin 22. This circuit is armed by three gates which are generated on 1A4. They are the tracker power gate at 1A8 pin 21 (fig. 2-33, zone A1) (HI from Ts to Ts +20 seconds), the IR intensity gate at pin 20 (zone A4) (goes HI at Ts +17.0 seconds) and the IR power inhibit gate at pin 32 (zone A1) (goes HI at Ts +1 second). Connector pins 12 or 14 are LO whenever the TTS mode switch (S6) is in the boresight or self test position. In the boresight or self test mode the U8B output is held LO by the LO output from U4A for 1 second and then returns HI. At Ts +17 seconds the U8B output will switch LO and will return HI at Ts +20 seconds. In the trainer mode the U6B output will be locked HI. In the missile command mode the U6A output will be LO and the U8B output will only respond to the U4A output.

(d) IR monitor gain select. This circuit is located on 1A10A1 (fig. 2-35, zone D2, D3) with its output at P1-40. The circuit input, seen at P1-28 (zone D1) is fed from P1-22 on 1A8 (fig. 2-33). U7 is a noninverting driver.

(e) Test sample decode logic/filters hold gate. This circuit is located on JA10A1 (fig. 2-35, zone C2, C3) with its output at P1-23 (zone C1). The input at P1-24, which is a HI switching LO level at Ts +12 seconds and then returning HI at Ts +13 seconds, is inverted by U3A and then switches flip-flop U4 at Ts +13 seconds when the inputs at U4, pin 2 goes LO. At this time U4 pin 6 goes HI and U4 pin 9 goes LO. The output waveforms at U5D is as shown on figure 2-35.

(4) IR pulse stimulus generator/IR pulse sample gate. This circuit is located on 1A4A2 (fig. 2-29, zone C6, C7) with its output at P1-6 (zone D1). The 8 msec output from counter U2 (zone A7) is fed to U16 pin 1. This pulse will occur initially at Ts +8 msec and stays HI for 2 msec and then will reoccur every 10 msecs. U16 is a one-shot multivibrator that will produces 20 usec width positive (HI) pulse at pin 8 whenever a negative-going pulse is applied to the input on pin 1 (zone C6). Since the pin 1 input pulses every 10 msec, the output at pin 8 will be a 100 Hz, 20 usec pulse chain. This pulse is armed at Ts +10 seconds by U17B and is inhibited at Ts +11 seconds which is seen at U17B pin 12. The output is seen at U17A.

g. UUT Stimuli Parameters. This system is located on 1A2 (fig. 2-27), 1A3 (fig. 2-28), and 1A4 (fig. 2-29). The associated wiring is shown on figure 2-25 for the monitor unit and figure 2-37 for the OAF.

(1) Tracker power. K5 on 1A2A1 (fig. 2-27, zone D3) controls the + and - 13 Vdc power to the UUT. When in the boresight, missile command or trainer test modes between Ts and Ts +20 seconds (tracker power gate at P1-31, fig. 2-27, zone D2) the U2 output (zone D2) is approximately +12.5 Vdc which actuates K5 (zone D3). + and - 13 Vdc is fed through K1, P1-30 and 27 (fig. 2-25, zone A13) J1-L and M (fig. 2-25, zone B10), OAF J1-L and M (fig. 2-37, zone B1), OAF J3-2 and 3 (fig. 2-37, zone 62) to the UUT. At Ts +20 seconds, U2, pin 4 (fig. 2-27, zone D3) goes LO which switches the U2 output LO and drops out K5.

(2) Cam solenoid inhibit driver (CSI). The cam solenoid inhibit gate is generated on 1A4, P1-16 (fig. 2-29, zone B9) and then fed to card 1A3 U6 (fig. 2-28, zone C2). In the foresight mode, U6 will be armed and the output will be a +12.3 Vdc pulse between Ts +18.4 sec. and Ts +20 seconds. This output is fed out monitor unit J1-K (fig. 2-25, zone B10) through OAF J1-K (fig. 2-37, zone B2) and energizes OAF K1 (zone B2). This applies +13 Vdc to pin 1 on the UUT connector J3 (zone B2).

(3) First motion discrete (FMD). This UUT stimuli is developed by the FMD gate on 1A4 pin 3 (fig. 2-29, zone D9) which is a HI level going LO at Ts +250 msec. This voltage step is driven by U5 on 1A3A1 (fig. 2-28, zone C2). The U5 output, which is a +12.3 Vdc going LO at Ts +250 msec, is fed out monitor unit connector J1-P (fig. 2-25, zone B10), through OAF connector J1-P (fig. 2-37, zone B1) to the UUT connector J3-5 (zone B2).

(4) Frequency select. In the boresight test mode, the ground on 1A3A1 pin 8 (fig. 2-28, zone D1) holds U4D (zone D2) output HI. At this time, a voltage divider

is established by R25, VR3 (16 volt zener), and R28 with a -11.6 Vdc output seen at Q6 base (zone D3). With -13 Vdc at the emitter, Q6 is forward biased. Q6 conducts, feeding -12.7 Vdc through the monitor unit connector J1-U (fig. 2-25, zone B10), OAF connector J1-U (fig. 2-37, zone B1) to the UUT through J3-9 (zone B3). When in any TTS mode except boresight, the U4D output (fig. 2-28, zone D2) will be LO which shorts the VR3 cathode to ground. Since VR3 is a 16 volt zener, the entire -13 Vdc is dropped across it which leaves a zero voltage drop across R28 (zone D2) and cuts off Q6. When the UUT is connected, approximately +12 Vdc will be seen at 0AF J3-9 (fig. 2-37, zone B3). When the UUT is disconnected, J3-9 will be an open.

h. Trigger Output. This circuit is located on 1A7 (fig. 2-32) and the OAF. The associated wiring is shown on fig. 2-25 for the monitor unit and on figure 2-37 for the OAF.

(1) This test verifies that the UUT trigger output energy, during trigger actuation, when expended into a 1.25 ohm load, is greater than 17.0 millijoules and that the trigger pulse width is less than 10 mseconds.

(2) The test is performed by firing the UUT trigger energy into a 1.25 ohm load in the OAF, (fig. 2-37). This 1.25 ohm load consists of wire resistance, UUT/ OAF connector J3 contact resistance (zone B3) and resistor R4 in series with the parallel combination R6 and R9. This resistance is calibrated by adjusting R6 until the series resistance between J3 pin 15 and 14 (zone B3) is exactly 1.25 ohms. When the UUT is fired into the load, current flows through these resistances. As the energy current flows through R4 a voltage is developed across it. This voltage is fed out of the OAF through J1-a and J1-b (zone B4) to 1A7 (fig. 2-25, and fig. 2-32) to differential amplifier AR1 on 1A7A2 (fig. 2-32, zone D6). AR1 amplifies the energy pulse voltage by -2.74 and then feeds the output to squaring amplifier U1 (zone C6). This output is then integrated by AR2 (zone C7).

(3) The timing circuit for evaluation of the pulse width of the trigger energy envelope, is initiated by the AR1 output (zone D6). This output will switch comparator U2 when the input voltage envelope to AR1 exceeds 117 mVdc and will then arm gate U3D allowing the trigger output timing pulse to activate switch U4 (zone D8). The U2 output also is fed through U3C and the RS circuit (U8A/U8B) (zone B6) to arm (HI) U8C allowing the 10 kHz pulse to be fed through to U9 and U10 (The 10 kHz comes from the master counter on 1A4). The purpose of U9 and U10 is to produce a 8 msec pulse which switches flip-flop U7 when the TTS mode switch is in the trigger output position [enables U3A output (HI)]. The output is a 10 msec pulse

(because the pulse width is 2 msec and U7 switches on the negative going pulse) which is fed to gate U3D. The output of U3D will be LO as long as the input pulse (to AR1) is still above 117 mVdc and if the time period is less than 10 mseconds. As soon as the input pulse decays, voltage comparator U2 will switch LO and U3D will switch HI. If the 10 msec timing pulse times out before the trigger pulse decays, U3D output will switch HI. The positive pulse from U3D switches U4 on. When U4 switches, a ground is fed to the AR2 integrator which stops integration and tries to return the integrated pulse to zero. The integrated pulse amplitude is fed to voltage comparator U5. If the trigger output pulse is greater than 17 mil joules and $\leq$ 10 msec wide, the U5 output will switch LO and then be stored by U6. The trigger output status is fed out through pin 8 of 1A7. In summary, the integrater will continue to integrate for the pulse width or until 10 msec has elapsed. The voltage height of the integrated output is fed through the U5 peak detector for a final status.

j. IR Source Control Voltage Generator System. This circuit is located on 1A8 (fig. 2-33). The associated wiring is shown on figure 2-25. This system generates the IR source control voltage that stimulates the IR source current generator. This system generates both the training and the tactical modulating frequencies. In the TTS missile command mode the IR output is at the tactical modulated frequency. This frequency is manually selected by the operator on the frequency switches S4 and S5 (fig. 2-25, zone B38) which are coded for security. The S4/S5 digit switches on the TTS monitor panel will select or generate 100 discrete frequencies over the frequency band.

(1) High frequency oscillator. This circuit is a crystal oscillator consisting of quartz crystals Y1, Y2 or Y3, amplifiers Q1, Q2 and output drive transistor Q3 on 1A8A2 (fig. 2-33, zone A6 to A8). The crystal operating current is developed through R14 (zone A7) crystal (Y1) through U9B (zone A6) to ground. The series crystal resonating frequency is amplified by Q1 and Q2. R22 and R23 are stabilizing resistors connected to bypass capacitors C6 and C7. These circuit components prevent regeneration. Output driver Q3 feeds the counter circuit (U11D). The frequency of this circuit is established by the crystal selected. In this circuit, one of the three crystals may be selected to develop 9.6 MHz for the center frequency signal (crystal Y1, zone A6), 9.936 MHz for the high frequency signal (crystal Y2, zone A6), and 9.264 MHz for the low frequency signal (crystal Y3, zone A6. Each of these crystals are switched on by logic circuitry.

(a) Center frequency. In the boresight test mode only the Y1 crystal is used. At this time, a HI is seen at inverter U14C (zone B6) Input. The LO output drives U16B, U16A, U14A and U14D outputs HI. This turns off crystals Y2 and Y3 and applies a HI to both U9B (zone B6) Inputs driving its output LO and enabling crystal Y1. In the missile command test mode, a ground is applied at inverter U14C (zone B6) input. The U14C HI output arms gates U16B, U16A, U14A and U14D. Prior to Ts + 13.1 seconds and after Ts +16.0 seconds, the U16B, U16A, U14A, and U14D outputs will be HI. This turns on crystal Y1 and turns off crystals Y2 and Y3 as discussed above.

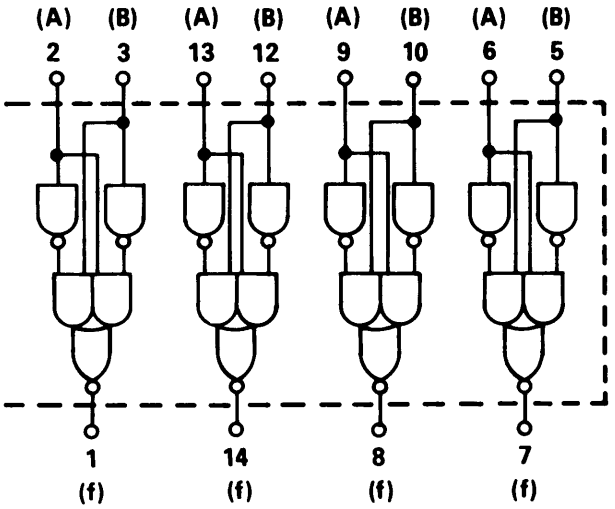
(b) High and low frequency. At Ts +13.1 seconds the IR high frequency gate at P1-10 goes HI. The gate is developed on 1A4 with the output at P1-30 (fig. 2-29, zone D1). This HI produces a LO at U14D and U16A (fig. 2-33, zone A5, A6) outputs, and a HI on U9B output. This turns crystal Y1 (center frequency) off and Y2 (high frequency) on. At Ts +14.50 seconds the IR high frequency gate at U14D input goes HI and the IR low frequency gate at U14A input goes HI. This turns off crystal Y2 and turns on Y3. By shifting from one crystal to another, the oscillator output frequency will shift +3.5 percent and -3.5 percent about the center frequency.

(2) Decade frequency select switch. S5/S4 (fig. 2-25, zone C38), located on the front panel of the TTS monitor panel, is a decade-to-binary coded decimal switch used to decode the tactical frequency. This switch is divided into units and tens with the truth tables being as shown below.

UNITS DIAL POS.	BIT 1	BIT 2	BIT 4	BIT 8
0				
1	LO			
2		LO		
3	LO	LO		
4			LO	
5	LO		LO	
6		LO	LO	
7	LO	LO	LO	
8				LO
9	LO			LO

(3) IR source frequency decode circuit for use in TTS missile command mode. This circuit is located on 1A8A2 (fig. 2-33) and consists of a decode comparator circuit, missile command arming circuit, decade counter circuit, reset circuit, and frequency deviation circuit.

(a) Decode comparator circuit. The four outputs from switch S4 and S5 (fig. 2-25, zone C38) are fed to 1A8 P1 through P8. (Fig. 2-33, zone D1) to inverters U1D, U1C, U1B, U5D, U5C, U5B, U5A (zone B5, C5) which inverts, switches outputs, and enables (HI) or disables (LO) the individual U2, U3, or U4 digital comparator circuits (zone B6, B7). The following simplified schematic and truth table is provided to assist in understanding the operation of the U2, U3, or U4 comparator.



TRUTH TABLE		
A	B	f
0	0	1
1	0	0
0	1	0
1	1	1

A simple way to follow the circuit is to assume that a HI on pin 3, 12, 10 or 5 on U2, U3, or U4, enables the logic level coming from the decade counter. As an example, if the output of U1A (zone C5) is a HI and U1B, U1C, or U1D are LO, the output from U2 would be the same signal as the U6 pin 11 (zone C6) output which is the 9.6 MHz output of the high frequency oscillator divided by 8 on a LO going HI signal at 0.8 usecond after reset. The U2, U3, and U4 summed outputs (pins 7, 8, 14 and 1 on each pack) are fed through two divide by two flip-flops U12 and U13 for the selected frequency output at U17C, pin 8 (zone D6). To summarize, the U13 flip-flop output frequency is determined by the position of the binary switches on the monitor panel.

(b) Missile command arming circuit. In the missile command mode the frequency decode circuit is armed to produce the tactical frequency. In this mode

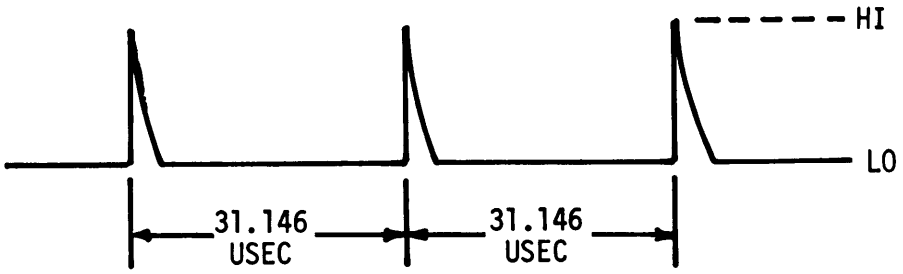
a ground is fed to inverter U14C (zone B6). The U14C output arms the U11A gate (zone D5) allowing the output to be fed back to reset counters U6, U7, and U8 through U11A.

(c) Decade counter circuit. The decade counters U6, U7, and U8 on card 1A8A2 operates in the same manner as the master TTS counter on 1A4. With the 9.6 MHz center frequency clock pulse applied to counters U6, U7, and U8 (zone C6, C7, C8), their outputs, seen on pins 11, 12, 13, and 14 will be as shown in figure 2-41.

(d) Reset circuit and operational example. The following example is given to assist in understanding the system. Assume the S4/S5 digit switch inputs to card 1A8 are as follows (fig. 2-33, zone D1):

UNITS	BIT	1, P1-1	APPLY LO
UNITS	BIT	2, P1-2	APPLY HI
UNITS	BIT	4, P1-4	APPLY HI
UNITS	BIT	8, P1-3	APPLY LO
TENS	BIT	1, P1-8	APPLY LO
TENS	BIT	2, P1-7	APPLY HI
TENS	BIT	4, P1-5	APPLY HI
TENS	BIT	8, P1-6	APPLY LO

With the TTS mode switch in missile command and the test start switches initiated, the U11A gate (zone D5) will be enabled (HI on pin 1) and U11D will be feeding a 9.6 MHz square wave clock pulse to the U6, U7, and U8 counters. At this time we will assume the clock pulse to be on center frequency of 9.6 MHz. With counters U6, U7, and U8 operating, their outputs are fed to 4 bit comparators U2, U3, and U4. Using the truth table shown in paragraph 2.4 j (3)(a) we determine the U2, U3, or U4 comparator outputs. The comparator outputs are sunned together and a composite positive pulse is received when all subpulses go high, which will occur at 29.9 usec after reset. If there was no reset to the counter, the second pulse will occur at 69.9 usec and so on. As soon as the comparator output pulses are all HI, U11A output goes LO which is fed to the counter reset line and resets the U6, U7, and U8 counters. As soon as the reset occur (LO) the counter sequence will start over. The U2, U3, U4 comparator output for the example would be as shown here.



This output is fed through U12 flip-flop which switches on every negative swing and then through U13. The U12 output will be a 16.054 kHz square wave and the U13 output will be a 8.026 kHz square wave. During this test mode, the trainer frequency reset circuit U9A, U18B, and U18A (zone D7) outputs are held HI. In the TTS missile command mode at Ts +13.10 sec and at Ts +14.50 sec the counter output frequency, at U17C (zone D6) will shift up 3.5 percent from center frequency and then down 3.5 percent from center frequency. This frequency shift occurs when the oscillator shifts from crystal Y1 (zone A6) to Y2 and then Y3 (zone A6).

(4) IR source frequency decode circuit for use in TTS boresight mode.

(a) Boresight mode. In the boresight mode, this system develops a training frequency of 5.0 kHz. At this time a HI from TTS mode switch S6 is applied at inverter U14C input (fig. 2-33, zone 6B). The LO U14C output drives U11A output HI which disables the missile command tactical frequency reset path from the U2/U3/U4 comparator outputs. For the boresight mode, the operation of the decode comparator circuit and the decode counter circuit is the same as was discussed above for the missile command mode. Since the reset circuit is the key to this system it will be discussed in detail.

(b) Reset circuit and operational example. In this mode prior to Ts +13.1 sec or after Ts +16.0 sec the U9A gate (fig. 2-33, zone D7) will reset the counter at 100 usec after the first reset pulse. The following example is given to assist in understanding this system.

1. Assume the TTS S4/S5 digit switches (fig. 2-25, zone B38) are still set as described in the missile command example above. In this mode the counters will continue to count until a reset is given (LO to pin 9 on U6, U7, or U8) and the only source of reset is from U9A, U18B or U18A (zone D7). Prior to Ts +13.1 sec or after Ts +16.0 sec U9A is enabled and U18B and U18A are disabled. The inputs to U9A are as follows:

U9A pin 2,	2.083 usec
U9A pin 1,	4.166 usec
U9A pin 5,	10.416 usec
U9B pin 4,	83.330 usec
	99.995 usec

The U9A output will be a HI going LO pulse at 100 usec which will reset the counters. At this time the counters will reset, which will phase each U9A input LO again and switch the U9A output HI, which removes the reset. This reset pulse from the U9A output will then switch LO every 100 usec.

2. After this first reset, the U2, U3, U4 outputs will pulse HI at 31.14579 usec and then pulse again at 69 usec when the U2, U3, U4 outputs again become coincident. This second pulse results because the counter is continuously counting. Then at 100 usec the U9A output resets the counter and the process is repeated. This results in a waveform out of U2, U3, and U4 comparators as shown in line A in figure 2-42. The important thing to note in this example is that two positive pulses will occur at the U2, U3, U4 output every 100 usec. Flip-flop U12 (zone D5) which switches on the declining edge of each positive pulse, has an unsymmetrical output whose period is 100 usec as shown in line B in Figure 2-42. Flip-flop U13, which also switches on the declining edge of each positive pulse has a symmetrical square wave output period of .200 usec or 5.0 kHz (training frequency).

3. At Ts +13.1 seconds (elapsed time from master counter on card 1A14) gate U9A (zone D7) is disarmed by a LO at pin 3 and U18B (zone D7) is armed by a HI at CR2 (zone D6) cathode. At this time U18B adds its inputs as follows:

U18B pin 13,	83.333 usec
U18B pin 12,	8.333 usec
U18B pin 9,	.833 usec
U18B pin 10,	1.0416 usec
	93.5406 usec

4. This results in a negative pulse out of U18B every 93.541 usec which resets counters U6, U7, and U8. This will produce a nonsymmetrical square wave, with a period of 93.541 usec, at the output of flip-flop U12 (zone D5). Flip-flop

U13 output will be a symmetrical square wave with a period of 187.082 usec or 5.345 kHz.

5. At Ts +14.5 seconds (elapsed time from master counter on card 1A4) gate U18B (zone D7) is disarmed by a LO at pin 11 and gate U18A (zone D7) is armed by a HI at CR3 cathode. At this time U18A adds its inputs as follows:

U18A pin 5,	1.0416 usec
U18A pin 4,	2.0830 usec
U18A pin 1,	104.1666 usec
	107.2912 usec

6. The U10 (zone D7) pin 6 output, which is the input of U18A pin 1, switches HI when the U10 input pulse goes LO. The U10 input is fed from counter U8 pin 11, which is LO for 83.33 usec, and then goes HI for 20.83 usec. This results in the U10 output switching HI at reset + 104.160 (83.33 + 20.83) usec. With the U18A inputs described above, the output will go LO at 107.285 usec which will reset counters U6, U7, and U8. This will produce a nonsymmetrical square wave with a period of 107.285 usec at the U12 flip-flop output (zone D5). The U13 flip-flop output will be a symmetrical square wave with a period of 214.58 usec or 4.660 kHz. This reset circuit provides this frequency shift for use in the UUT filters test.

(5) IR source DC reference generator.

(a) In all modes, this circuit develops a reference voltage for the AC voltage generator.

(b) The output at the Q2 emitter (fig. 2-33, zone D4) will vary with the OAC temperature. This output voltage will be 5.0 Vdc at ambient temperature (77°F) and will vary from 3.0 to 7.0 Vdc with temperature.

(c) The AR1 pin 3 (zone D3) reference voltage from the R8 wiper is set at approximately 2.5 Vdc. The AR1 gain resistances consists of R5, R9, R10, and thermistor RT1 on the OAC (fig. 2-39, zone C2). Q2 is an output drive transistor.

(6) AC voltage generator. The output from the reference voltage generator, is scaled through R25 (fig. 2-33, zone B5), R27 (zone B5), R28, and R29 with the output being developed between R25 and R27 and applied to AR1 pin 3 (zone B6). The IR source frequency square wave output from U17C (zone D6) is summed with the reference voltage at the AR1 pin 3 input. In the boresight test mode the U20A and U20B outputs are HI (the output drive transistor in these gates are open collector

type), and if the ambient temperature is 77°F, the AR1 (zone B6) output will be a 0 to 5.496 VP-P square wave pulse. In the missile command mode at Ts +13.1 see, the U20B output goes LO which decreases the voltage divider to R25, R27, and R28 and decreases the AR1 output square wave pulse to 4.998 VP-P. At Ts +14.5 seconds the U20B output will go HI and the U20A output will go LO, reducing the voltage divider to R25 and R27 and changing the AR1 output to 4.520 VP-P. AR1 has a gain of 2.

(7) Control voltage filter and sealing. This circuit takes the square wave output from AR1 on 1A8A2 (fig. 2-33, zone B6) and filters it into a useable sine wave.

(a) Training frequency low pass filter. In the boresight test mode the AR1 square wave output (fig. 2-33, zone B6) is at the training frequency of 5.0 kHz. This signal is filtered into a sine wave by AR3 a low pass filter. In this mode the U15 (zone B7) output at pin 1 enables (HI) the AR2 output and U15 pin 7 inhibits (LO) the AR3 output. The AR3 output is fed into voltage divider R25, R26, R28, R29, and R31. The input from the divider to AR4 (zone B3) will be a 1.25 VP-P sine wave with a 5.00 VP-P sine wave (at 77°F) at the AR4 output.

(b) Tactical frequency low pass filter. In this mode the AR1 (zone B6) output, which now is at the tactical frequency, is attenuated by R18 (zone B2) and then filtered into a sine wave by the AR2 filter circuit (zone B2). In this mode the U15 (zone B7) outputs switch to a LO at pin 7 and to a HI at pin 1, which shorts out the training frequency filter AR3 output and enables (HI) the AR2 tactical frequency low pass filter output. The AR2 output is fed through voltage divider R20, R21, R28, R29 and R31 with the AR4 output being 5.0 VP-P.

(c) Missile command squelch. In the missile command mode at Ts +17.0 seconds, the U3C (fig. 2-33, zone B3) output switches HI for 1.4 seconds which turns on switch U5 (zone C3) and drives potentiometer R29 wiper LO. This new ground reduces the R20, R21, R28 and R29 voltage divider by 85 percent. The AR4 output now becomes approximately 0.750 VP-P. The AR4 output is fed out card 1A8 pin 13 to OAF J1- D (fig. 2-37, zone B4) and card 2A1 pin 10 (fig. 2-38, zone A2).

k. IR Stimuli System. The IR source control voltage, discussed in the previous paragraph, is fed to the IR source current generator on the OAC 2A1 card (fig. 2-38). This generator provides the operating current plus the modulating signal for the IR radiating diodes in the OAC. The IR radiating diodes in the OAC are sensitive to temperature variation. The diodes are most efficient at low

temperature, becoming less efficient as the temperature rises. To compensate for this variation, above nominal current is fed through the diodes at high temperatures (above 77°F) and less than nominal current is fed through the diode at low temperature (less than 77°F). The IR source control voltage from (fig. 2-33) carries the temperature compensating information to the IR source current generator circuit AR1, AR2, and AR3 (fig. 2-38). When the OAC temperature is high the sine wave amplitude at 2A1 pin 10 will be above 5.0 VP-P and will be less than 5.0 VP-P when temperature is low. This input sine wave voltage will vary from 3.0 VP-P to 7.0 VP-P. The AR2 (fig. 2-38, zone A3) DC level generator, converts this increase or decrease in sine wave amplitude to a dc level which increases or decreases the Q1/Q2 (fig. 2-38, zone A4) condition, changing the IR diode current flow.

(1) IR source current generator. The IR source control voltage out of 1A8, pin 13, (fig. 2-33) is a 5.0 VP-P (nominal) sine wave at the 5.0 kHz training frequency when in the boresight test mode or at the tactical frequency when in the missile command mode. This signal is fed out J1-d on the monitor unit (fig. 2-25, zone C39), through OAF J1-d (fig. 2-37, zone B4) to pin 10 on 2A1 (fig. 2-38, zone A2). This input is buffered by AR1 (fig. 2-38, zone A2) and then fed to the dc level generator circuit which sums the input sine wave with two dc levels. The first dc level is a bias voltage developed from the +13 Vdc, which is amplified by the AR2 circuit with scaling resistors R3 and R5 (gain = .037). The second dc level is developed by CR1 (zone A2) rectification of the 5.0 VP-P sine wave which is filtered by C2 and amplified by the AR2 circuit with scaling resistors R4 and R5 (gain = 0.562). The sine wave is amplified by the AR2 circuit with scaling resistors R2 and R5 (gain = 0.562). The AR2 output is nominally a 2.81 VP-P sine wave riding about a minus 1.61 Vdc level. This minus voltage is amplified by AR3. It forward biases Q1 and Q2 which allows current flow from emitter to collector.

(2) IR diode current flow. There are four combinations of IR diode paths.

(a) Near-center diode at low intensity. In this mode K1 (zone B3, B4) is deenergized, for low intensity, and Q4 is forward biased for the on-center IR diode selection. The IR diode current is from 2A1 ground, through P1-14, through OAF J1-R (fig. 2-37, zone D3) to 3A1 pin 3 (fig. 2-39, zone C5) and to R11, R12, and R13 (zone C3). Current out of R11, R12, and R13 is fed out 3A1 pin 1 (zone D5) through OAF J1-N (fig. 2-37, zone D3) through 2A1, P1-12 (fig. 2-38, zone A2), through K1 contact A, through Q1 and Q2, through forward biased Q4, through K1 contacts B, through R17 and out P1-20 (zone C2). Current is then fed out OAF J1-L

(fig. 2-37, zone D3) through OAC near-center diode CR1 (fig. 2-39, zone C2), through 3A1 pin 8 and fuse F1 to -13 Vdc power at 3J1-H (zone B6). At this time the current fed through the IR diode results in an IR intensity output of 1.84 ± .46 $x10^{-10}$ watts/cm^2.

(b) Near-center diode at high intensity. In this mode K1 will be energized. The actuation of this relay is discussed in a later paragraph. The IR diode current is now from ground through 2A1 P1-14 (fig. 2-38, zone A2), through OAF J1-R (fig. 2-37, zone D3), through 3A1 pin 3 (fig. 2-39, zone C5), through R15, R16, and R17 (zone C4), through 3A1 pin 4 (zone D5), through OAF J1-M (fig. 2-37, zone D3), through 2A1 P1-13 (fig. 2-38, zone A2) to K1 contact A (zone A4). The remaining current path is as discussed above. This results in a higher IR diode intensity output of 4.26 13.34 X 10^{-8} watts/cm^2.

(c) Off-center diode at high intensity. In this mode Q4 (fig. 2-38, zone B4) will be reversed biased and Q3 will be forward biased. The control of these transistors will be discussed in a later paragraph. In this mode, instead of current flowing through Q4 as discussed in the previous paragraph, current will flow through Q3 and out P1-19 (zone B2), through OAF J1-19 (fig. 2-37, zone C5), through OAC to IR off-center diode CR2 (fig. 2-39, zone C2), through CR2 to fuse F1 on 3A1 which is at -13 Vdc. The result is the IR near-center diode being turned off and the off-center diode radiating at 0.885 ± 0.754 x 10^{-7} watts/cm^2 intensity.

(3) IR diode selection circuit. When the source select gate input at 2A1 pin 18 (fig. 2-38, zone B2) is HI, U3 output is LO and the U2 output is +13 Vdc which forward biases Q4 and reverse biases Q3, which turns the near-center diode CR1 (fig. 2-39, zone C2) on. When the source select gate at pin 18 (zone B2) goes LO the U2 output goes LO and the U3 output switches to +13 Vdc which forward biases Q3 and reverse bias Q4, which turns the off-center diode on.

(4) IR diode intensity select. When the IR intensity select gate input at 2A1 pin 11 (fig. 2-38, zone B2) is LO, the U4 (zone B2) output will be +13 Vdc which will actuate K1 and increase the IR diode current. When the P1-11 input is HI the U4 (zone B2) output will be LO and K1 will deenergize.

(5) Test modes. In the boresight, missile command, trainer, and self test modes, the P1-18 and P1-11 input, which programs the proper test setup, will be as shown on Figure 2-38, flag notes 4 and 11.

(6) IR pulse current generator circuit. The purpose of this circuit is to inject a 250 ma pulse into the near-center diode at the same time that the diode is

operating at LO intensity and being modulated by the tactical frequency. This 250 ma current is modulated by a 100 Hz square wave pulse train. The on time is 20 usec for each pulse. The 250 ma current source is regulated but will vary approximately 6 percent over the temperature range. The near-center diode current is developed across R17 on 2A1 (fig. 2-38, zone B4) which is fed to and differentiated by AR4 on 2A1A1. The amplified AR4 output (gain = 15), which is a modulated sine wave equal to 10 times the diode current, is rectified by AR5 and then forward biases the Q5 drive transistor to this dc level. The current flow through R33 develops approximately 3.8 Vdc which is fed back to AR5 to maintain the proper AR5 output and Q5 current. The 3.8 Vdc is used as the plus power for the IR pulse current generator by being fed across R37. The current through Q7, R38, and the near-center diode is approximately 0.250 ma.

m. Dynamic Gain. The circuitry for this system is located on 1A9 (fig. 2-34) and 1A3 (fig. 2-28) with associated wiring shown on fig. 2-25 and fig. 2-37. This system evaluates the UUT vertical and horizontal rate position outputs during an IR position shift to the UUT optics. In the TTS foresight mode at Ts +19 seconds, the TTS OAC IR output to the UUT is shifted from a line of sight position (or boresight position) to an up and to the right position. At this time, the UUT vertical and horizontal rate outputs, at UUT connector pins 10 and 11, shall respond with a dc voltage shift of $\geq$ 4.5 Vdc (or voltage level shift) in vertical and $\geq$ 6.1 Vdc in horizontal. The UUT outputs, which are seen at OAF J3 pins 10 (vertical) and 11 (horizontal) (fig. 2-37, zone B3), are inverted by AR1 and AR4 on 1A9A2 (fig. 2-34, zone C6) and fed to 1A3 pins 6 and 11 (fig. 2-28, zone B1). AR1 and AR4 on 1A9A2 become unity gain buffers when connected to the UUT, because of a 1.0K UUT output impedance. These inverted outputs from 1A9 are fed through 1A3, P1-6 and P1-11 to the U8 switch (zone B6) on 1A3A2. When the dynamic hold gate input at U8 pins 9 and 13 (zone B6) is HI, the inverted horizontal and vertical rate position signals are fed through U8. Since the vertical and horizontal dynamic gain evaluation circuits on 1A3A2 are nearly identical only the horizontal circuit will be discussed.

(1) Horizontal dynamic gain evaluation circuit. The inverted horizontal UUT rate position signal, prior to Ts +19.0 see, as seen at U8 pin 7 (fig. 2-28, zone B6) is filtered by R6, R7, C3, and C4 (zone B6) to a dc level, which is then stored by C4 (zone B7) and amplified by AR1 (gain = +2). This AR1 sample and hold output is compared with the horizontal rate position signal, seen at 1A3A2-J10 by amplifier AR2. When the AR2 output is greater than +5 Vdc, the U7 output will switch

HI. At Ts +19 seconds the dynamic hold gate, at U8 pin 9 and 13, goes LO turning switch U8 off and allowing no more signal current to flow through it. At this same time the IR input to the UUT has been shifted which will cause the UUT horizontal rate position output signal at 1A3A2-J10, to increase in the negative direction. AR2 then compares this new horizontal rate position voltage level with the stored AR1 sample and hold voltage level. If the voltage at 1A3A2-J10 is equal to or more negative than 6.1 Vdc, the U7 output at pin 7 will switch HI. Since the horizontal rate input to card 1A3 is a negative pulse, the U7 output will remain HI for only as long as the pulse stays more negative than 6.1 Vdc.

(2) Dynamic gain logic.

(a) The second half of this circuit verifies with logic that the U7 (fig. 2-28, zone B8) and U9 (zone B8) voltage comparators are only HI between Ts +19.0 and Ts +19.2 seconds. The U7 and U9 outputs compared with the dynamic gain hold gate, at P1-14 (zone C1) which is a HI from Ts +19.0 to Ts +19.2 seconds, by U1C and U1D (zone C6, D6). The outputs will be LO if both signal and gate are coincident. The vertical dynamic gain output is stored by U2C/U2D and the horizontal dynamic gain is stored by U2A/U2B.

(b) At Ts +19.5 seconds, the TTS verifies that the inverted rate pulse at 1A3A2-J10 and J2 has decayed to a level of less than -6.1 Vdc for horizontal and less than -4.5 Vdc for vertical. At this time the U7 and U9 outputs are compared with the dynamic gain low gate at P1-13 (zone D1), which is HI from Ts +19.5 to Ts +19.6 seconds. If the pulses are coincident the U1A (zone D6) or U1B outputs would be LO, which constitutes a no-go. In a go situation the U1A and U1B outputs will be HI and U3C output will be LO. This output is stored by RS circuit U3A and U3B (zone D7).

(c) In the boresight test mode a HI (enable level) will be fed to U4A pin 4 (zone D7). At the U4A input all the stored logic levels are compared. In a go situation all inputs will be HI driving U4A output LO. The circuit output is seen at U6 pin 9 which is a JK flip-flop and fed out P1-4 (zone C1).

(d) In the missile command test mode a LO is seen at U5C (zone D3) input pin 9 driving the output HI which is compared with a positive pulse from U4B at U5B. The U5B LO output is stored by U6.

n. Vertical Pulse System. The circuitry for this system is located on 1A5 (fig. 2-30) with the associated wiring shown on figure 2-25 and figure 2-37. This system evaluates the UUT vertical guidance wire pulse output during a boresight or

missile command test for pulse amplitude, pulse width, and first pulse occurrence. The vertical guidance wire signal from the UUT is fed through OAF J3-6, through the cabling and monitor unit to 1A5 pin 40 (fig. 2-30, zone C1). The input pulse train is buffered by AR1 (zone C2) which has a high capacitive input (C1 and C2) to simulate the actual missile guidance wire capacitance. In the discussions that follow, the leading edge of the P1-40 input vertical guidance wire pulse will be referred to as t = x and the trailing edge will be referred to as t = x + w.

(1) Pulse amplitude circuit. The pulses out of buffer AR1, are fed to voltage comparator U7 (zone C3) which conducts when the P1-40 input voltage exceeds 7.9 Vdc. U3B (zone B4) compares the U7 output with the vertical pulse sample gate, at P1-11 (zone B11), and the sample window from U2C (zone B3), which is a gate that is HI from 1.0 to 8.0 msec (t= x to t = x + w) after the leading edge of the first positive pulse seen at P1-40 (zone C1). When the three U3B (zone B4) inputs are coincident (HI) the output will switch LO and the status will be stored by the RS circuit U4D/U4C. The U4C pin 8 output will be LO if the input pulse amplitude, at P1-40 is less than 7.9 Vdc (for a no-go).

(2) Pulse width circuit. AR1 buffer (zone C2) also feeds pulse width comparator U9 (zone C3). This comparator will switch (output goes HI) when the input pulse at P1-40 exceeds +5 Vdc. At the trailing edge of the P1-40 input pulse (t= x + w) the U9 output will return low, which will produce a 3 usec positive pulse at the U8A (zone C4) output. U3A (zone C4) compares this U8A pulse output with the vertical pulse sample gate, from P1-11, and a test window from U6A/U6B outputs which is HI for 9 msec after the occurrence of the leading edge of the P1-40 input pulse (t = x). In a no-go situation (pulse width is less than 9 msec) the U3A output will switch LO and be stored by U4A and U4B.

(3) First pulse delay circuit. The U1OD output, which is LO for the period that the P1-40 input pulse is above 5.0 Vdc (t = x + w), produces a positive 6.6 usec pulse at t + x. U10A (zone A2) compares the U11B output with the first pulse delay gate at P1-15, which is a HI from Ts +250 msec to Ts +701 msec. In a no-go situation the U10A inputs would be coincident (HI) and the output would switch HI. In a go situation, the first vertical guidance wire input pulse at P1-40 has not occurred prior to Ts +701 msec and the U10A output will be HI. This status is stored by RS circuit U12D and U12C (zone A2). In a go situation, the first input pulse at P1-40 will occur between Ts +701 msec and Ts +748 msec. At this time, in the foresight or missile command test modes, the U8B inputs will be coincident (HI)

and the output will switch LO and this status will be stored by RS circuit U12A and U12B.

(4) Vertical pulse summing circuit. U13B (zone A4) sums the stored status of the pulse amplitude, pulse width, and first pulse occur circuits. If all circuits are go, the U13B inputs will be HI, the output will switch LO and be fed out P1-13 (zone A1).

p. Vertical Error System. The circuitry for this system is located on 1A5 (fig. 2-30) with the associated wiring shown in figure 2-25 and figure 2-37. This system evaluates the UUT vertical guidance wire repetition rate (vertical error) during the boresight and missile command test modes. The circuit input is at 1A5 pin 40 (fig. 2-30, zone C1).

(1) Vertical error counter circuit. This timing circuit utilizes 4 BCD counters, U1, U2, U3, and U4 on 1A5A2 (fig. 2-30, zone A5, A6, A7). The clock input for the counters is taken from the 10 kHz oscillator on 1A4, P1-20 (fig. 2-29, zone A1). This 5 volt digital, 10 kHz symmetrical square wave is buffered by U18B on 1A5A1 (fig. 2-30, zone A4) and then fed to pin 2 of counters U1, U2, U3, U4 (zone A5, A6, A7).

(a) Counters. The U1, U2, U3, U4 BCD counters function in the same manner as the master counter on 1A4 (fig. 2-29). The individual counter module outputs are LO going HI digital outputs at the times, from counter reset, shown on the figure 2-30 schematic (zone A5, A6, A7). The U1, U2, U3, U4 module outputs are on pins 11, 12, 13, and 14.

(b) Counter reset. The reset for the U1, U2, U3, U4 counter modules is a negative 3.3 usec pulse which will occur 3.3 usec after t + x. This means that the card 1A5 vertical error counters will reset 3.3 usec after the leading edge of each P1-40 input pulse. The U11B output (zone C4), which was discussed in the vertical pulse paragraph, is a positive 6.6 usec pulse which occurs at t + x. The U11A output switches LO 3.3 usec after its input switches HI. U11A is the reset output.

(2) Vertical error logic control and decode circuits. The individual parameters are as follows:

(a) Vertical pulse trigger. This output is a 6.6 usec pulse which occurs at t + x.

(b) Reset pulse. It should be noted that this reset is not the same as the counter reset discussed above. The U10D (fig. 2-30, zone C3) output, which was previously discussed, is a HI going LO pulse at t+ x and remaining LO until t =

x + w . This output is delayed by U14A (zone B2) and U14B (zone B3) and produces a U10B output that goes from HI to LO 30 usec after t = x + w and remains LO for 3 usec.

(c) Sample pulse. The U10D (zone C3) output discussed above is delayed by U15A and U15B to produce a 3 usec positive pulse, 14 usec after t = x + w.

(d) Boresight low decode. U6B (zone C7), which combines the LO going HI 4.0 and 0.8 msec signals from counters U1 and U2, produce a LO output at Ts +4.8 msec. U7 (zone C8) is a JK flip-flop with an and gate- input at pins 3 and 4. The clock input on U7 is pin 2. When the 300 msec input at U7 pin 3 goes HI and the U6B input to U7 pin 2 goes LO the U7 pin 6 output will switch HI. This results in a LO going HI pulse at counter reset +304.8 msec for boresight low decode. At t = x +3.3 usec (the leading edge of the next input pulse at P1-40), the counter reset will again occur, which resets all counter (U1, U2, U3, U4) outputs back to LO. This reset pulse is also fed to U7 pin 5, which resets the pin 6 output back to LO. After the reset is removed (3.3 usec) the counter will begin to count down and the steps will be repeated. This will occur from Ts to Ts +21 seconds of the timed sequence.

(e) Boresight HI decode, missile command LO decode, missile command HI decode, squelch LO decode, and squelch HI decode. Each of these circuits is equivalent to the boresight LO decode circuit discussed in paragraph (d) above, so they are not discussed here individually. The individual circuit outputs are shown on the figure 2-30 schematic, zone C8 and D8. It should be noted that the U8, U12, and U16 outputs are taken from pin 9 ($\overline{Q}$ output) so their reading will switch from HI to LO.

(3) Vertical error boresight circuitry. This circuit verifies that in the boresight test mode the UUT vertical guidance wire pulse repetition rate, at P1-40 (fig. 2-30, zone Cl) is between 2.32 and 3.28 PPS which corresponds to a PRT of 304.9 msec to 431.0 msec.

(a) Gate U17D on 1A5A2 (fig. 2-30, zone B5) sums the boresight LO decode and the boresight HI decode logic levels to provide a test window (enable period) at the U17D output that is HI going LO at counter reset +304.8 msec and then returning HI at counter reset +431.0 msec. In the boresight test mode the U17D output is inverted by U17C. The U24B (E6) output is held HI by a LO at input pin 5, which is fed from the TTS mode switch. In a go situation, the next vertical pulse will occur in the U17C, (zone C6) boresight window. At this time, the vertical pulse trigger pulses HI and all U22B (zone C6) inputs become coincident, driving its

output LO. This status is stored by RS circuit U24D and U24C and fed to U25B. At t = x + w +30 usec the U24D and U24C RS circuit is reset which returns its output HI.

(b) U25B is armed by the P1-2 (zone D1) test sample gate. In a go situation, a LO out of the U24D and U24C circuit will latch the U25B output HI for a go. In a no-go situation the output will be HI. When the sample pulse occurs, the U25B inputs will be coincident and the output will switch HI for a no-go. This output is stored by U26A and U26B. In the boresight or missile command test mode at Ts +12 to 13 seconds the U25A inputs will be coincident (HI) when the vertical pulse trigger switches HI and its LO output will be stored by RS circuit U26C and U26D (zone C7). If a P1-40 input pulse is missing, the U27B output will go LO at reset +600 msec for a no-go. In a go situation the 400 msec pulses from the counter circuit will never time out and the U27B output will stay HI. The missing pulse timing is stored by U13B and U13A. When all U27A inputs are HI the output will switch LO for a go.

(4) Vertical error missile command. This circuit verifies that when the TTS is operating in the missile command mode the UUT vertical guidance wire pulse repetition rate, at P1-40 (zone C1) is between 5.78 and 11.80 PPS which corresponds to a PRT of 84.8 msec to 173.0 msec. Gate U24A SUMS the missile command LO decode and the missile command HI decode from U10 and U12 (zone D8) to provide a HI going LO test envelope at counter reset +84.8 msec to counter reset +173.0 msec. With the TTS mode switch in missile command the U17C output will be forced HI, by a ground at pin 9, and U24B will be enabled by a HI at U24B pin 5. C7 (zone C6) is for noise suppression. The remaining portion of this circuit is the same as was discussed above in paragraph 2-4 p. (3). The circuit output status (LO for GO) is fed out of this card on P1-3 (zone D1).

q. Horizontal Guidance Wire Ripple.

(1) The circuitry for this system is located on 1A6 (fig. 2-31) with the associated wiring shown on figure 2-25 and figure 2-37.

(2) This system evaluates the ripple level on the UUT horizontal guidance wire when the TTS is in the boresight or missile command test modes. The system also verifies that the 20 Hz ripple is in the GO region of 86 mv to 662 mv peak.

(3) The signal from the UUT is fed through 0AF J3-7 (fig. 2-37, zone B7) through the cabling and the monitor unit to 1A6 P1-9 (fig. 2-31, zone B2). C6 and C8 (zone C9), which block the dc signal component and allows only the ac component to pass through. These capacitors cause a slight differention of the input signal,

which is compensated for in circuit gain.

(4) AR4 (zone C10) which is a high pass amplifier with a gain of 15, filters out the higher frequency noise so that only the 20 Hz ripple will be evaluated. U6 and U10 (zone C11) compare the AR4 output with a reference voltage. U10 is scaled by R24 and R25, to switch HI when the P1-9 (zone B2) input ripple exceeds 86 mv peak. U6 will switch HI when the P1-9 input ripple exceeds 662 mv peak. In a go situation the input ripple at P1-9 will be greater than 86 mv peak but less than 662 mv peak which will leave the U6 output LO and switch the U10 output HI.

(5) In the boresight or missile command test modes at Ts + 12 seconds the test sample gate at P1-7 (zone D2) will be HI which will make all of the U11A (zone C12) inputs HI, driving its output LO. At this time U6 output is LO driving the U7A output HI. The U7A and U11A outputs are stored by RS circuits U8A and U8D, U8B and U8C, and summed by U9B. The status of the U8B and U8C output arms (HI) the horizontal error gate U9A when the ripple input at P1-9 is greater than 86 mv peak. In a no-go situation the P1-9 ripple input will be greater than 662 mv peak, which makes both U7A inputs HI, driving its output LO. This is seen as a HI output at U9B (zone C13) for a no-go.

r. Horizontal Error. The circuitry for this system is located on TTS monitor unit card 1A6 (fig. 2-31) with the associated wiring shown on figure 2-25 and figure 2-37. The horizontal error circuit evaluates the UUT horizontal guidance wire output level while in the boresight and missile command modes. The circuit input is at 1A6 pin 9 (fig. 2-31, zone B2) as discussed for ripple evaluation.

(1) Horizontal error, boresight. This circuit verifies that when the IR input to the UUT optics is on line of sight (or boresight), the horizontal guidance wire dc output will be 0 Vdc ± 0.824 Vdc. The horizontal input P1-9 (zone B2) is filtered and amplified by the AR1 (zone A10) circuit to produce a dc level output equivalent to the average level of the P1-9 ripple input. Voltage comparators U1 and U2 (zone A15) compare the AR1 output voltage with a reference voltage selected by R2 and R4 (zone A11). The U1 output will switch LO when the AR1 output is more negative than -824 mVdc. In a go situation, when the dc component of the P1-9 input is between -824 mVdc and +824 mVdc the U1 and U2 outputs will be HI which will switch the U12D (zone D10) output LO. In this mode U12A pin 1 input is HI and U12B pin 5 input is LO. This produces a LO at the U11B output and a HI out of the U7C and U7D RS circuit. If the ripple input level is greater than 86 mv peak, the U8B and U8C RS circuit output will be HI. With both U9A inputs HI the output will switch LO for a horizontal error system go. In a no-go situation the U11B output

(zone D11) will be HI. At Ts +12 seconds to Ts +13 seconds the P1-7 test sample will go HI, switching U7B LO and U9A output HI for a no-go.

(2) Horizontal error hold circuit. This circuit is located on 1A6A2. In the boresight test mode, the UUT IR input from the OAC should produce a UUT horizontal guidance wire dc output of 0 Vdc. Due to tolerances in the UUT and the TTS IR and optics input, this exact zero voltage is not achievable. Since the exact horizontal error dc voltage at boresight (or line of sight) is not exactly zero, this error voltage needs to be added to or subtracted from the horizontal error dc level when the IR input to the UUT has been moved to the missile command position (which is 2.36 MR off of boresight, in the vertical and horizontal plane). The horizontal error hold circuit on 1A6A2 stores the horizontal wire dc voltage during the boresight mode tests. When the missile command test is run, the stored error voltage will be added to the missile command error voltage. This summed voltage is then used for the missile command horizontal error evaluation.

(a) Horizontal hold boresight mode. In the foresight mode, K1 (zone 12B) is energized and K2 is deenergized which allows the horizontal error dc output from AR1 (zone A10) to be stored on C3 (zone A12). K1 is only energized from Ts +12 seconds to Ts +13 seconds when the test sample gate at U5A pin 1 (zone B11) is HI. A LO U5A output actuates K1.

(b) Horizontal hold, missile command mode. In the missile command mode U5B output (zone BJ2) goes LO, actuating K2. With K2 energized, AR2 buffers the dc voltage stored by C3 (zone A12) and establishes the AR3 pin 2 (zone B14) reference voltage.

(3) Horizontal error, missile command. This circuit verifies that when the IR input to the UUT optics is in the missile command position (off boresight), the horizontal guidance wire dc output will be between 3.77 Vdc and 5.15 Vdc above the boresight horizontal dc error reference. The horizontal error voltage is fed out of AR1 (zone A10), as was done in the boresight mode and applied to the noninverting input of differential amplifier AR3 (zone B14). The AR3 output will be the difference between the hold circuit voltage and the missile command error voltage times the AR3 gain of -0.825. U3 and U4 (zone B15) compare the AR3 output voltage with a reference voltage selected by R11 and R13. The U3 output will switch LO when the AR3 output is greater than 5.15 Vdc. U4 output will switch LO when the AR3 output is less than 3.77 Vdc. In a go situation, when the dc component of the P1-9 input is between 3.77 and 5.15 Vdc and the boresight reference voltage on C3

(zone A12) is 0 Vdc, the U3 and U4 outputs will be HI which will switch the U12C output LO and the U11B output LO for a go status. The remaining logic is as was discussed for the boresight mode.

s. Wire Clamp. The circuitry is located on 1A5 (fig. 2-30) and 1A6 (fig. 2-31) with the associated wiring shown in figure 2-25 and figure 2-37. The wire clamp circuitry evaluates the UUT clamp function on the vertical and horizontal guidance wire outputs.

(1) Horizontal guidance wire clamp circuit. In this system the TTS performs two test functions. First, the TTS verifies that there are no time varying signals greater than + or - 500 mv peak on the UUT horizontal guidance wire between Ts and Ts +350 msec. Secondly, the TTS verifies that the UUT releases this clamp command between Ts +350 msec and Ts +650 msec. When the UUT clamp is removed the ripple will appear on the horizontal guidance wire.

(a) Horizontal guidance wire clamp delay circuit. The horizontal guidance wire signal is applied to pin 3 of AR5 (C14) and amplified. The nominal gain of AR5 is +10.5. Voltage comparators U13 and U16 (zone C15) compare the AR5 output voltage with the + and - 5 Vdc reference. The U13 output will switch LO if the AR5, pin 3 input voltage is higher than +500 mVdc and the U16 output will switch LO if the AR5, pin 3 input becomes more negative than -500 mVdc. During the wire clamp occur evaluation the U13 and U16 outputs must remain HI from Ts to Ts +350 msec for a go condition. This will switch U17A output LO. At this time (prior to Ts +350 msec) the horizontal clamp occur gate at P1-2 (zone D2) is LO and the horizontal clamp delay gate at P1-6, (zone C2) is HI. This arms the U14B (zone D14) input with a HI and disarms the U17B (zone D14) input with a LO. In the go situation discussed above, the U17A LO output will drive the U14B output HI for a go. In a no-go situation, (input P1-9 voltage is greater than + or - 500 mVdc) one of the U17A inputs will be LO, which gates the output HI. The two HI's at the U14B input drives its output LO which is stored by RS circuit U15C and U15B.

(b) Horizontal guidance wire clamp occur circuit. At Ts +350 msec to Ts +650 msec, the horizontal clamp occur gate goes HI and the delay gate goes LO which enables (HI) U17B (zone D14) and disables (LO) U14B, keeping its output (HI). In a go situation the UUT clamp will be removed and the P1-9 (zone B2) input will rise above +500 mVdc causing the U17A output to switch HI and the U17B output to switch LO. If the UUT is in a go status the U17D inputs will be HI, driving its output LO.

(2) Vertical guidance wire clamp circuit. This circuit is located on 1A5. In this system the TTS monitors the UUT vertical guidance wire output and verifies that no time varying signals greater than + or -500 mv peak occur between Ts and Ts +701 msec. The UUT vertical guidance wire signal is buffered by AR1 on 1A5A1 (fig. 2-30, zone C2) and then fed to voltage comparators U16 and U17 (zone D2 and D3). When the P1-40 input voltage exceeds +500 mVdc the U16 output will switch LO and when the P1-40 input voltage exceeds -500 mVdc the U17 output will switch LO. In a go situation the U16 and U17 outputs will be HI. At this time the P1-20 (zone D1) vertical clamp gate input will be HI which produces a HI at the U13A (zone D3) output and a LO out P1-12.

(3) Wire clamp composite circuit. The vertical clamp status at card 1A5 pin 12 (fig. 2-30, zone D1) is fed to card 1A6 pin 15 (fig. 2-31, zone C2). When the UUT vertical and horizontal clamp circuits are in a go status 1A6 U8A and U8B inputs will be LO which will produces LO at P1-16.

t. Trigger Safe. The circuitry is located on 1A7 (fig. 2-32) with associated wiring shown on figure 2-25 and figure 2-37. This system evaluates the UUT tracker trigger safing switch during a nontrigger actuation period to determine if the UUT safety short is across the UUT tracker trigger solenoid and if the short is of the proper resistance value. The TTS performs a resistance test, which verifies the UUT trigger safe resistance is equal to or less than 255 milliohms, and a transient test that verifies and impedance equal to a series RL network (605 microhenries and 300 millihom resistor in parallel with a 3000 pf capacitor) is unsafe. This test is performed by placing a current pulse through the UUT safing switch (and a parallel OAF resistance circuit) to ground. The voltage drop across the trigger safing resistance is evaluated for amplitude level.

(1) OAF load resistance. The OAF trigger load resistance at OAF J3 pins 14 and 15 (fig. 2-37, zone B3), is a resistive load which simulates the tracker battery squib. In the trigger output test, the UUT trigger energy is expended into this load. In the TTS trigger safe test, this OAF resistive load is in parallel with the UUT trigger safing switch. This OAF load is seen between J3-15 and J3-14 (zone B3) through R9 in parallel with R6 in series with R4 (zone C4). In the trigger safe test, current is fed in at J1-Z (zone B4) through the OAF resistive load in parallel with the UUT trigger back to power ground at J1-F (zone B4).

(2) Trigger safe current generator. This circuit is located on 1A7A1 (fig. 2-32) and is a 252 ma constant current device. This current source is developed

from the -13 Vdc power. The generator output is applied out P1-37 through the monitor unit and cabling to the OAF resistive circuit of R4, R6, and R9 (fig. 2-37, zone B4). The generator is regulated by amplifier AR2. It maintains the voltage drop across R19 the same as the reference voltage across VR1 by controlling the base voltage of Q2 to increase or decrease current flow. Prior to Ts +20.15 seconds the current generator is held off by Q3 which shorts the Q2 base to -13 Vdc (the delay generator will be discussed in a later paragraph) when a negative going pulse is fed to the cathode of VR2. Since VR2 is a 16V zener it will absorb all of the -13 Vdc from the bus leaving zero voltage across R18. This will cut-off Q3, removing the -13 Vdc from the Q2 base allowing current to flow to the load.

(3) Trigger safe delay generator. This circuit provides the test envelopes for the trigger safe dc test and the trigger safe transient test. U5 (zone A2) is a one-shot multivibrator which produces a positive 0.5 second pulse output when the dynamic gain low gate, at P1-27 (zone A2) switches LO. U6 is a JK flip-flop which will switch when the input goes LO. The U6 output will be a LO going HI step at Ts +20.1 seconds. U4B and U7A are time delay devices which will produce a HI to LO step at Ts +20.1 seconds + 8 usec. The U7A output will produce a 30 usec positive pulse (due to C7) at Ts +20.1 seconds +10 usec. The dc test envelopes at the output of U8A (zone A3) is provided by U7B and U8A in the same manner as above. The U8A output will be a 15 usec positive pulse at Ts +20.1 usec. The U6 output will also drive the U9D (zone A2) output LO (when the testing gate at P1-23 is HI) which drives the VR2 cathode LO, turns off Q3 (zone D3) and allows the current generator to turn on.

(4) Trigger safe dc test. This test verifies the UUT trigger safe resistance is less than 255 milliohms. At Ts +20.1 seconds the trigger safe current generator, applies 252 ma out P1-37 of card 1A7 (fig. 2-32, zone C1) through the monitor unit and cabling, through OAF J1-7 (fig. 2-37, zone B4) to the OAF R4, R6, and R9 (zone B4) in parallel with the UUT to ground at P1-F (zone D3). If the UUT trigger safe resistance is 255 milliohms R4 will develop a 76.3 mVdc drop across it. This voltage drop is fed out OAF J1-pins A and B to 1A7 pins 21 and 32 (fig. 2-32, zone C1). This voltage drop is amplified by AR1 (zone C3) and fed to voltage comparator U2• In a go situation the UUT trigger safe resistance will be less than 205 milliohms and the U2 output will be LO. In a no-go situation this output will be HI. This output is compared with dc test detection gate, from the U8A (zone A3) output to U9B. In a no-go situation the U2 output will be HI which will be coincident

with the U8A output driving the U9B output LO. This LO is fed through U8B and U9C and switches U10 to a HI output for a no-go.

(5) Trigger safe transient test. In the transient mode, the UUT verifies the tracker trigger output is not an inductive impedance. If the tracker trigger does exhibit an inductive load, there will be a large current surge for a short period of time when the current generator is turned on. The current will decay when the inductance has been overcome. The voltage drop across R4 in the OAF follows the current change and is reflected at the output of differential amplifier AR1 (fig. 2-32, zone C3). The output is fed to voltage comparator U1 (zone B4). The U1 output goes HI when the trigger output reflects the current envelope surge (the voltage equivalent across the trigger output load under these conditions will be equal to or greater than approximately 200 rev). The U1 output is compared with the transient test detection gate at the U3B gate. If the transient comparator (U1) output is HI during the transient test detection gate at U7A output (zone A3), the U3B gate output will switch LO (no-go). If there is no transient pulse at the AR1 input, the U1 output will be LO (go) and U3B output will be HI (go).

(6) Trigger safe final summing circuit. At Ts +20.1 seconds in the boresight or missile command test modes, if the trigger safe dc test and the transient test outputs at U1 and U2 (zone B4, C4) are LO, the U8B inputs will all be HI and the U8B output will go LO. The output status will be stored by U10 (zone A4).

u. IR Pulse System. The circuitry for this system is located on 1A9 (fig. 2-34), and 1A10 (fig. 2-35) with associated wiring shown on figure 2-25 and figure 2-37. Between Ts +10 seconds and Ts +11 seconds in the missile command test mode, the IR pulse stimuli is superimposed on the IR modulated output. In this system the TTS evaluates the UUT vertical and horizontal rate position outputs on pins 10 and 11, between Ts +10 and Ts +11 seconds, to verify that the TTS OAC generated signal does not cause the UUT to false sample. The TTS monitors the UUT vertical and horizontal rate position outputs to verify that there are no false samples greater than 1.0 volt peak at the output of a derate circuit. Since the vertical and horizontal false sample detectors are nearly identical, only the vertical will be discussed here.

(1) False sample detectors. The UUT output seen at OAF J3-10 is fed to 1A9 (fig. 2-34) and inverted by AR1 on 1A9A2 (zone C6). This output is derated by R3, R4, C3, C4, C1, R5 (zone C6) and amplified by AR2 (zone C7). Voltage comparator U1 switches LO (for a no-go) when the derated signal output exceeds +5 Vdc. U2 will

switch LO when the derated signal output exceeds -5 Vdc. In a go situation, comparators U1, U4, U2, U5 will all have a HI output and the U3 output will be LO. It should be noted that the UUT false sample pulse is approximately 50 msec in width so the U3 output in the case of a no-go will be a positive pulse approximately 50 msec wide or less.

(2) IR pulse logic. U3 logic output on 1A9A2 (fig. 2-34, zone C8) is fed through 1A10 pin 13 (fig. 2-35, zone A1) to U8C and U10C (zone A2). In the missile command mode, if a no-go input is received from U3 on 1A9A2 (fig. 2-34, zone C8) it can only shift the U8C output (fig. 2-35, zone A2) during the 1.0 second HI output period of the IR pulse sample gate seen at P1-14 (zone A1). Any U8C output no-go is stored by RS circuit U8A and U8B. In the boresight, trainer, or self-test mode the U8D pin 10 input will be HI. This input is compared with the IR pulse sample gate at U8D and the output switches LO when the IR pulse sample gate switches. This keeps RS circuit U8A and U8B output HI. This assures a go when in the boresight, trainer, or self-test modes regardless of signal input. The IR pulse output is at U9A.

v. Filter test system. The circuitry for this system is located on 1A10 (fig. 2-35) with associated wiring shown on figure 2-25 and figure 2-37. This circuit verifies that the UUT sum and difference output signals are attenuated 2 db when the UUT IR input from the OAC is shifted in frequency by ± 3.5 percent. This test is performed in both the boresight and missile command test modes.

(1) Logic conditioning circuit. For the operation of this TTS test circuit, it is necessary to discuss various logic circuits.

(a) Sample and hold relay driver voltage. At Ts + 13 seconds the test sample decode at P1-24 (fig. 2-35, zone C1) returns HI which switches U3A and JK flip-flop U4 producing a LO to HI output at pin 6. At this time both U12A (zone B3) inputs are HI driving its output LO, resulting in a HI being fed from the U14 output on 1A10A1 (zone B4) to actuate K1 on 1A10A2 (zone B6).

(b) AGC and filters mode select. This logic level at U1 pins 9 and 13 (zone A5) will be HI from Ts to Ts +16 seconds. This HI activates the U1 switch and shorts pins 8 and 7 and pins 1 and 14 which shunts R2 (zone A5) and R21 (zone B5) and makes the circuit input scaling equal to one.

(c) Sum and difference peak detector discharge circuit. Between Ts +13.1 seconds and Ts +14.5 seconds the IR high frequency gate at P1-18 (zone B1) goes HI and is inverted by U15B. Prior to Ts +16 seconds the U13 output (zone B2) will be

HI. This results in U15D going HI and U16B pulsing LO at Ts +13.1 seconds. The U16B output is a 25 msec positive pulse which is inverted by U17A and U17B and fed to R8 (zone A6) at the AR1 output and R27 (zone B6) at the AR3 output. At Ts +16 seconds (the IR high frequency gate at P1-18 has already gone LO) the U13 (zone B2) output switches LO which steps U15D HI and U15C LO producing a second 25 msec pulse at the U16B output and a negative pulse at the U17B/U17A output. These negative pulses are programed at the beginning of the filter evaluation test (Ts +13.1 seconds) and at the beginning of the AGC test (at Ts +16.0 seconds) to discharge the peak detector filter capacitors C4 (zone A9) and C9 (zone B6).

(2) Filter evaluation circuit. The sum and difference signals out of the UUT are fed to pins 4 and 5 on 1A10 (fig. 2-35). Since the sum signal path and the difference signal path is nearly identical, only the sum signal will be discussed here. C1 removes any dc component and feeds the signal to the AR1 circuit. R2 is shorted by U1 (zone A5) at this time. The AR1 peak detector circuitry output is filtered by C4 and charges sample and hold capacitor C5 (zone A6). AR2 (zone A7) buffers the dc voltage at C5 and references U2 and U3 with this value. The AR2 output also feeds voltage divider R13, R14, and voltage comparator U4 (zone B7). At Ts +13.0 seconds, K1 on 1A10A2 (zone B6) is energized which opens the voltage path to C5. The AR2 output voltage remains the same. At Ts +13.1 seconds the IR modulating frequency to the UUT is increased by 3.5 percent. In a go situation, the UUT will respond with a sum signal that is 2 db down from the voltage prior to Ts +13.0 seconds. This lower amplitude voltage is seen at the AR1 circuit output (zone A6) which is fed to voltage comparator U4. If the U4 input is equal to or greater than the 2 db level, the U4 output will be HI for a go. In a no-go situation this output will be LO.

(3) Filter logic. In a go situation, the U11A inputs (zone C5) will be HI and the output will be LO. This U11A output is only sampled during either the high frequency test window (filters low sample gate) or the low frequency test window (filters high sample gate). The U11D or U11C outputs are stored by RS circuits U12A and U12B, U12D and U12C, then summed by U10A.

w. AGC Test System. The circuitry for this system is located on 1A10 (fig. 2-35) with associated wiring shown in figures 2-25 and 2-37. At Ts +17.0 seconds, in the boresight test mode, the OAC IR output switches to a high intensity IR level, which causes the UUT sum and difference output signals to increase to the AGC level. This system verifies the AGC sum and difference signals from the UUT to be between 8.2 and 20.0 VP-P. This test is only performed in the boresight test

mode.

(1) Logic conditioning circuit.

(a) Sample/hold relay driver. At Ts +16.0 seconds the U13 output (fig. 2-35, zone B2) switches HI. This results in the U14 (zone B4) output remaining LO and K1 (zone B6) remaining in the deenergized position for the remainder of the test.

(b) AGC/filters mode select. At Ts +16.0 seconds the U13 (zone B2) output switches LO and the U1 (zone A5) switch will open and remove the short across R2 (zone A5) and R21 (zone B5).

(c) Sum and difference peak detector discharge circuit. At Ts +16.10 seconds, a negative 25 msec pulse will be seen at the U17B and U17A (zone B3) output, which will discharge peak detector capacitors C4 (zone A6) and C9 (zone B6).

(2) AGC evaluation system. The UUT sum and difference signals through OAF J3 pins 12 and 13 (fig. 2-37, zone B3) are routed to 1A10, pins 4 and 5. Since the sum and difference circuits are identical, only the sum circuit will be discussed. The input signal is scaled by voltage divider R2 and R3 (zone A5) and fed to the AR1 (zone A6) peak detector circuit. The output, which is filtered by C5 (zone A6) and buffered by AR2, is compared with a reference voltage at U2 and U3 (zone A8). When the UUT output is less than 8.2 VP-P, the U3 output will switch LO. If the UUT output is greater than 20.0 VP-P the U2 output will switch LO.

(3) AGC logic. In a go situation all of the U8B (zone C5) inputs will be HI and the output will be LO. At Ts +17 seconds the OAC IR output switches to the AGC level which places the UUT in AGC and programs the sum and difference signals to the AGC level. At this time the AGC and squelch gate at P1-1 (zone A1), which goes HI for 1.4 seconds, is delayed 420 msec by U8A and produces a positive pulse output between Ts +17.42 seconds and Ts +18.4 seconds. This pulse arms U9B. In a go situation U9B output will switch HI and be stored by RS circuit U9D and U9C (zone C7). U10B is the circuit output. In a no-go situation one of the U8B (zone C5) inputs will be LO resulting in a LO at U9B output.

x. Squelch Evaluation System. The circuitry for this system is located on 1A5 (fig. 2-30), 1A6 (fig. 2-31), and 1A10 (fig. 2-35) with associated wiring shown on figure 2-25 and figure 2-37.

(1) Horizontal error squelch system. This circuit is located on 1A6A1 (fig. 2-31). When the OAC IR source drives the UUT into squelch this system verifies that the UUT horizontal guidance wire error dc voltage does not deviate more than ± 15

percent from the pre-squelch level. At the completion of squelch (Ts +18.4 seconds), the TTS verifies that the horizontal error voltage is in the go status. This system can be discussed in two parts.

(a) Horizontal error during squelch. In the missile command mode prior to Ts +17.0 seconds, the amplified horizontal error voltage is seen at the output of differential amplifier AR3 (fig. 2-31, zone B5). This error voltage is fed to voltage comparators U1 and U3 and to the sample and hold input resistor R18 (zone B3). Prior to Ts +16.8 seconds, the horizontal error dc voltage is stored in C7 (zone B4) through the A contacts of K2. AR3 amplifies the error voltage which appears across voltage divider R21 and R23. At Ts +16.8 seconds the K2 sample and hold relay (zone C4) is energized and the charge path of C7 (zone B4) is opened. With the input open, the AR3 circuit continues to produce the same output dc voltage. At Ts +17.0 seconds the UUT is driven into squelch. At this time, the horizontal error dc voltage at the AR3 output (zone B5) may shift plus or minus. If the new horizontal error dc voltage is higher than 15 percent of the dc voltage held on the sample and hold circuit, comparator U1 output will switch LO for a no-go. If the squelch horizontal error dc voltage is lower than 15 percent of the sample and hold voltage, comparator U3 output will switch LO for a no-go. The U1 and U13 outputs are summed with the AGC and squelch test gate, at P1-38 (zone C2), which goes HI at Ts +17.0 seconds and stays HI until Ts +18.4 seconds at U4B (zone D5). In a go situation the RS circuit U5A and U5D output will be a HI.

(b) Horizontal error after squelch. At Ts +18.4 seconds, the squelch command is removed and the TTS verifies that the UUT horizontal error returns to within the missile command tolerance values. This value is sampled between Ts +18.4 seconds and Ts +19.6 seconds. The horizontal error go or no-go status is taken from 1A6A2 U12B (zone D10) output. This output is inverted by U6D (zone D3) and compared with the P1-14, dynamic gain low gate, which is HI between Ts +19.5 and Ts +19.6 seconds, at U6C. In a go situation the U6C output will be HI and the U7C and U7D RS circuit output will be HI.

(2) Vertical error squelch system. This circuit is located on 1A5 (fig. 2-30). During the squelch period of Ts +17.0 and Ts +18.4 seconds, the TTS verifies that the UUT vertical error output seen at P1-40 (fig. 2-30, zone C1) goes to a preset PRT squelch level of 245.7 msec to 361 msec. That is, the time between the leading edges of any two pulses shall be 245.7 msec to 361 msec.

(a) Squelch, test pulse detection circuit. Gate U17A on 1A5A1 (fig. 2-30, zone B5) sums the squelch low decode and the squelch high decode logic levels to

provide a test window at the U17A output. This logic signal is a HI going LO level at counter reset (U11A output, zone C4) +245.7 msec and then returning HI at counter reset + 361 msec. At the leading edge of each vertical guidance wire pulse, (P1-40, zone C1) a positive 6.6 usec pulse (t=x +6.6 usec) (vertical pulse trigger) is seen at U18B input (zone B6) pin 5. This pulse is compared with the squelch test detection window at U18B pin 4. If the input signal is go, the U18B inputs will be coincident and the output will pulse LO. This output status will be stored by RS circuit U18D and U18C (zone B7). This RS circuit is reset by the reset pulse which occurs 3.3 usec after the leading edge of the input pulse (t = x +3.3 usec) at P1-40.

(b) Squelch test pulse occur circuit. The first reset pulse (U10B output, zone B3), which occurs after Ts +17.0 seconds, will switch the U21B output LO and set the RS circuit U21D and U21C. The U21D output will remain HI for the remainder of the test sequence.

(c) Squelch test pulse occur summing circuit. At Ts +17.0 to 18.4 seconds when the vertical guidance wire input pulses (at P1-40) are at a go PRT, the U22A (zone B7) output and the RS circuit U20C and U20D output will be HI for a go status.

(d) Squelch release pulse occur. At Ts +18.4 seconds the UUT is brought out of squelch. The first reset pulse (from U10B output, zone B3) that occurs after the UUT comes out of squelch will be coincident with the P1-7 (zone B1) squelch release gate and will switch the U23A (zone A7) output LO. This logic is stored by RS circuit U23D and U23C.

(e) Squelch release spacing circuit. The output from the RS circuit U24C and U24D (zone C6) switches LO when the vertical pulse trigger (from U11B, zone C4) occurs in the normal missile command decode window. This output is called the pulse spacing output and is fed directly to U19B (zone B6). Other inputs to the U19B gate are the squelch release gate at P1-7 (zone A1), the sampling pulse from U15B (zone B3), and the U23D and U23C output. In a go situation the U9B output will be HI. In a no-go situation the U19B output will switch LO and be stored by the RS circuit U20A and U20B.

(f) Vertical squelch summing. The vertical error squelch summing circuit consists of U19A. A LO output will constitute a go.

(3) Squelch false sample. During the squelch period, the TTS verifies there are no UUT false samples on the horizontal or vertical rate position outputs from the UUT. A false sample is defined as a voltage pulse that exceeds the average

value of the sampled pulses by more than ± 1.0 volt peak when read at the output of the TTS derate circuits. The circuitry is the same as was described for the IR pulse circuit except that the output of the false sample pulse summing gate U3, on 1A9A2 (fig. 2-34, zone C8), is through 1A10 pin 13 (fig. 2-35, zone A1) to squelch gate U1OC. This gate compares the false sample comparator output with the U10D output (which is the AGC and squelch gate from P1-1), whose leading edge has been delayed 102 usec by U11A. If no false samples are received during this time period, the U10C output will be HI for a go. This output is stored by the RS circuit U10A and U10B. The system output is at U9B.

(4) Squelch summing circuit. The squelch summing circuit is located on 1A6A1 (fig. 2-31). The composite gate U4B (zone D5) sums all of the previously mentioned squelch parameters. If all of the U4B inputs are HI, the output will be LO. The output is fed to U5C. This gate is enabled during the missile command mode. At this time the dynamic gain low gate at P1-14 (zone D2) occurs and a LO logic level will be seen at the output of U6B, (zone D7) which will set the RS circuit U8D and U8C and lock the U8C output LO which will also lock U5C output HI. The squelch status is fed out 1A6 P1-24.

y. Composite Summing Circuit. The circuitry for this system is located on 1A7 (fig. 2-32) and 1A10 (fig. 2-35) with associated wiring shown on figure 2-25. This circuit sums all of the individual system test status into one composite readout. The composite Band composite C outputs are seen at U12A and U12B on 1A7A1 (fig. 2-32, zone B3, C3). The composite outputs are fed to P1-25 and P1-26 on 1A10A1 (fig. 2-35, zone C1). The final summing gate is U2A on 1A10A1 (zone C4) with the main composite status being fed out P1-27 (zone C1).

z. Indicator Lamps. The intent of the testing lights are to give a status of the UUT during all periods of testing.

(1) At Ts the testing lamp illuminates and remains on until Ts +21 seconds. At this time, either the go or no-go lights will come on, depending on the logic status. The circuitry from the lamp control logic is on 1A3 (fig. 2-28) with the associated wiring shown on figure 2-25.

(2) The indicator lamp driver circuits, located on 1A3A1 (fig. 2-28), provide the lamp driving voltages for the function indicators.

(3) The TTS testing indicator will illuminate at T=O during any major test mode. In the self test mode, the testing, go and no-go indicators, via U4A, U3A and U3B on 1A3 (fig. 2-28, zone C3, D3), will illuminate and then extinguish 60

seconds later, as commanded by the inhibit-in-self-test circuit. This provides an indication of the function indicator lamp drivers and indicator lamps. In the trigger output mode, the testing indicator will extinguish when either a go signal from the UUT trigger evaluation circuit or a no-go signal from the normal lamp gate is received at U2C (zone C3).

(4) R20, R21, and R23 (zone C4, D4) provide isolation to monitoring test points. In the boresight or missile command mode, the go or no-go logic inputs are from the composite logic gate, through pole B of mode switch S6 (fig. 2-25, zone B2) through P1-18 of 1A3. In these modes, a go input will be through inverter U2D, gates U3C and U3B (fig. 2-28, zone C3) to lamp driver U7. U7 output will be HI from Ts +21 seconds to Ts +30 seconds, illuminating the go indicator with the testing indicator extinguishing at Ts +21 seconds, and the go indicator extinguishing at Ts +30 seconds. A no-go input in the boresight or missile command mode, is through U3D and U3A (fig. 2-28, zone C3, C4) to lamp driver U8. U8 output will be high from Ts +21 seconds to Ts +60 seconds illuminating the no-go indicator for this time period.

(5) The testing indicator will extinguish at Ts +21 seconds, and the no-go indicator at Ts +60 seconds. During this period, the mode switch can be rotated through the individual test positions and the go or no-go indicator will provide a status of the individual test. In the trainer mode of operation, the testing lamp will illuminate upon test start and extinguish upon test stop as commanded by the test start/stop switch. The go and no-go function indicators are not enabled during the trainer mode.

aa. Trainer Stimuli. The circuitry for this system is located on 1A8A1 (fig. 2-33) and 1A10 (fig. 2-35) with the associated wiring shown on figure 2-25. This system provides two parameters for the LET system checkout.

(1) Trainer mode, master clock inhibit circuit. In the TTS trainer mode at Ts +4 seconds, the logic input on P1-32 of 1A10 (fig. 2-35, zone C1) will switch from LO to HI. At this time 1A10A1 U6B inputs will be coincident and 1.5 usec later the U6B output will go LO. This LO is fed to P1-10 of 1A4 (fig. 2-29, zone B1) to inhibit the master clock and stop the counters.

(2) Trainer simulated trigger pulse. This circuit consists of a noise free positive step generator on 1A8A1 (fig. 2-33) and a signal conditioning circuit installed in the TTS trainer adapter cable. The trainer adapter cable conditioning circuit consists of one resistor and two capacitors. When a positive step occurs

at 1A8 P1-37 (zone C1) circuit output, the trainer cable conditioning circuit filters this into a positive energy pulse. The step generator for this circuit is located on 1A8A1 and consists of voltage comparator U2 (zone C2) and JK flip-flop U1 (zone C2). Prior to the TTS monitor panel trainer trigger switch actuation, the U2 pin 10 input is +5 Vdc which is stored on C1. The U2 inverting input at pin 1 is biased at 2.0 Vdc by voltage divider R2 and R40. At this time the U2 output will be HI. In the trainer test mode, when the TTS trainer trigger switch is actuated, a ground is placed on 1A8, pin 39 (zone C1). This ground discharges C1 (zone C2) lowering the U2 pin 10 input voltage to less than 2.0 Vdc and causes the U2 output to switch LO. This LO switches the U1 flip-flop (at pin 6) HI. This HI is then fed out P1-37 to the trainer cable signal conditioner circuit previously discussed. When the trainer trigger switch is released, the ground at P1-39 will be removed and C1 (zone C2) will again charge up to +5 Vdc and switch the U2 output HI. The next time the trainer trigger switch is actuated, the U2 output will again pulse LO, which will again switch U1 flip-flop output LO (and the P1-37 output LO).

(3) Trainer simulated sum signal. This circuit delivers a 29.0 mv 5kHz sine wave to the MTS. When the TTS trainer trigger switch is actuated and the trainer trigger gate goes HI, as discussed in the previous paragraph, this HI is also fed through 1A10 pin 36 (fig. 2-35, zone D1) to arm U6A (zone D2). At this time, U6A inverts the frequency stimulus square wave on P1-38. The AR1 filter amplifier (zone D4) filters the square wave into a sine wave. The AR1 output is attenuated by R6 and R7 and fed out P1-33 as a 290 mv RMS, 5kHz sine wave.

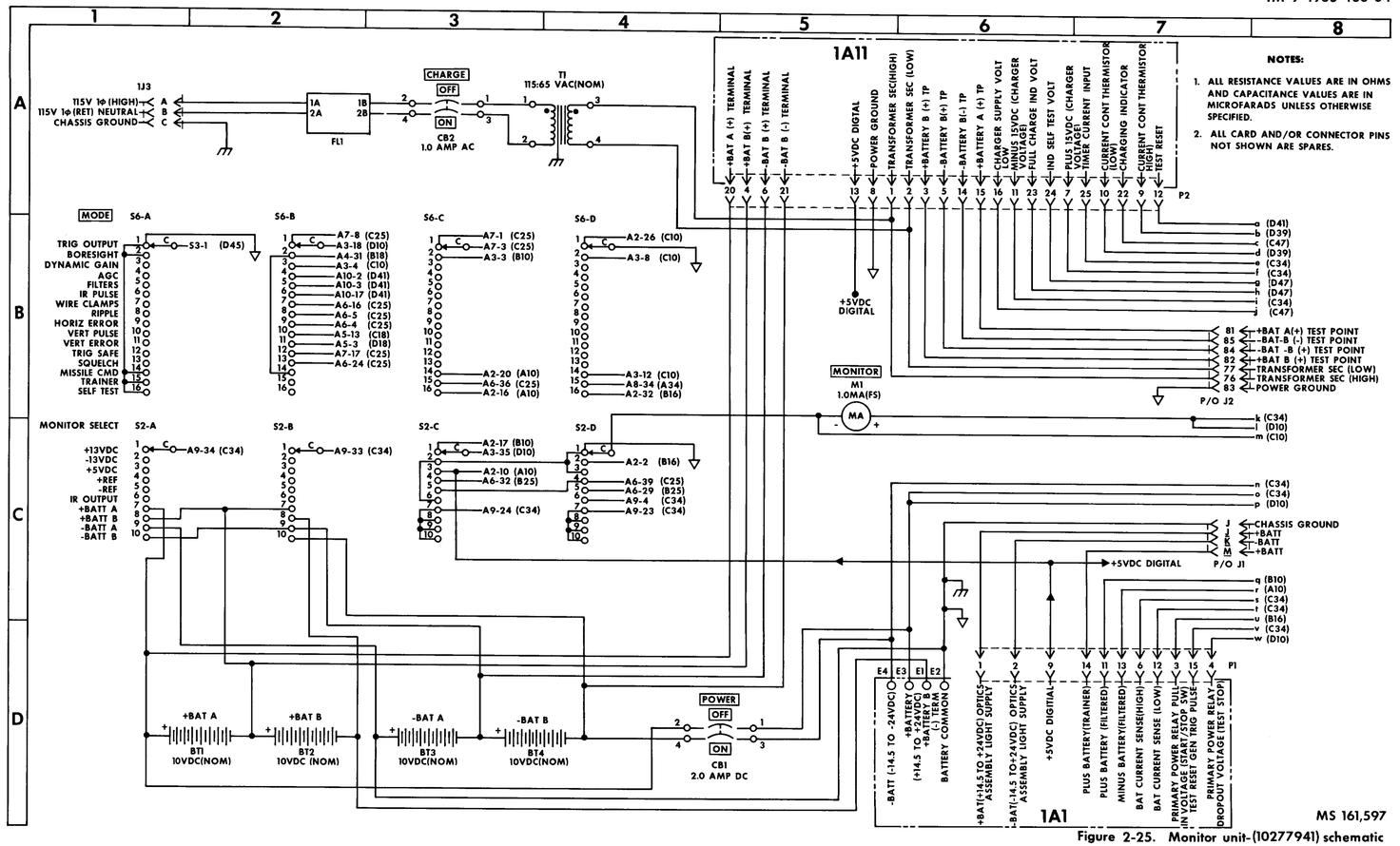


Figure 2-25. Monitor unit-(10277941) schematic diagram (sheet 1 of 6)

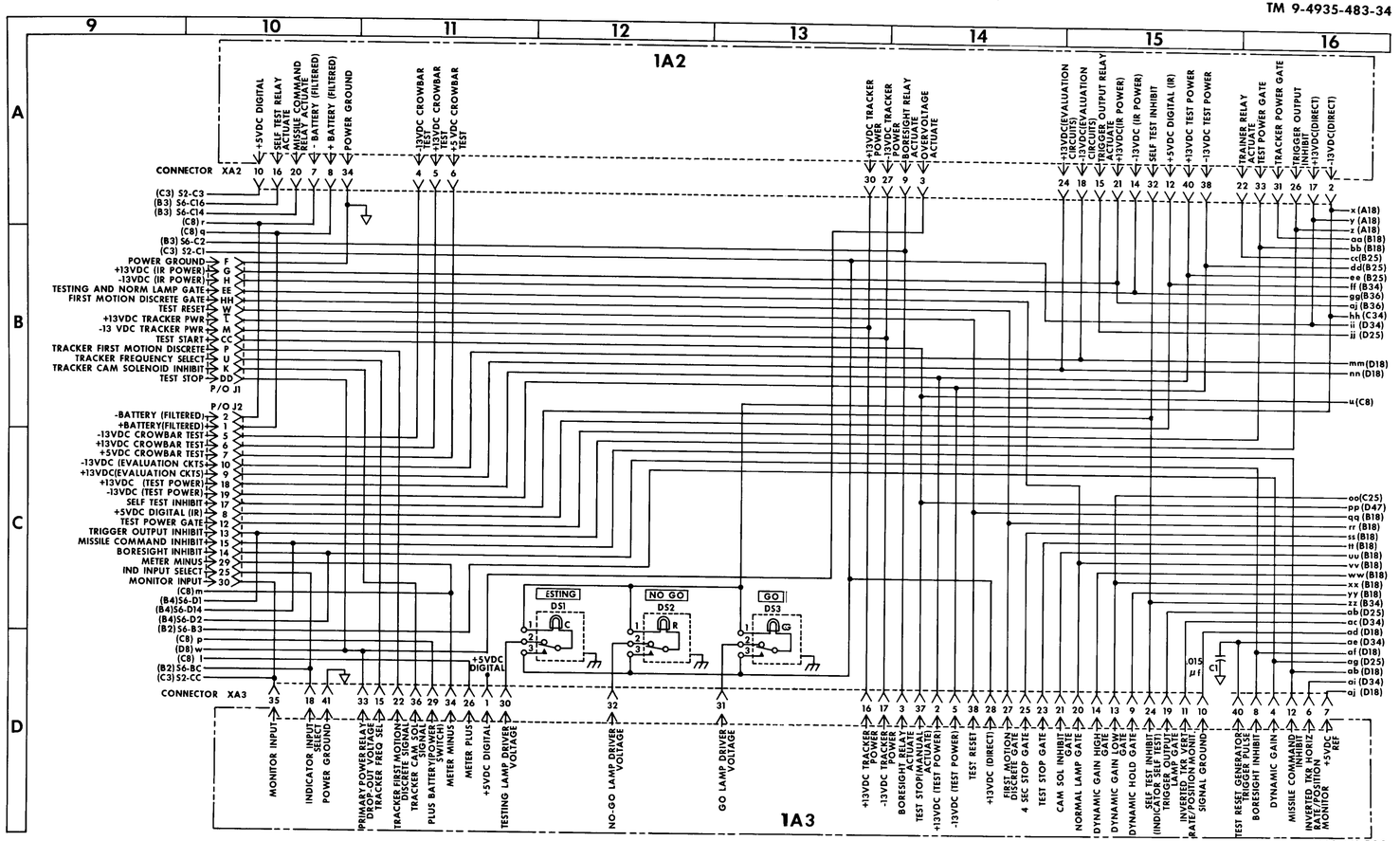


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Figure 2-25. Monitor unit (10277941) - schematic diagram (sheet 2 of 6)

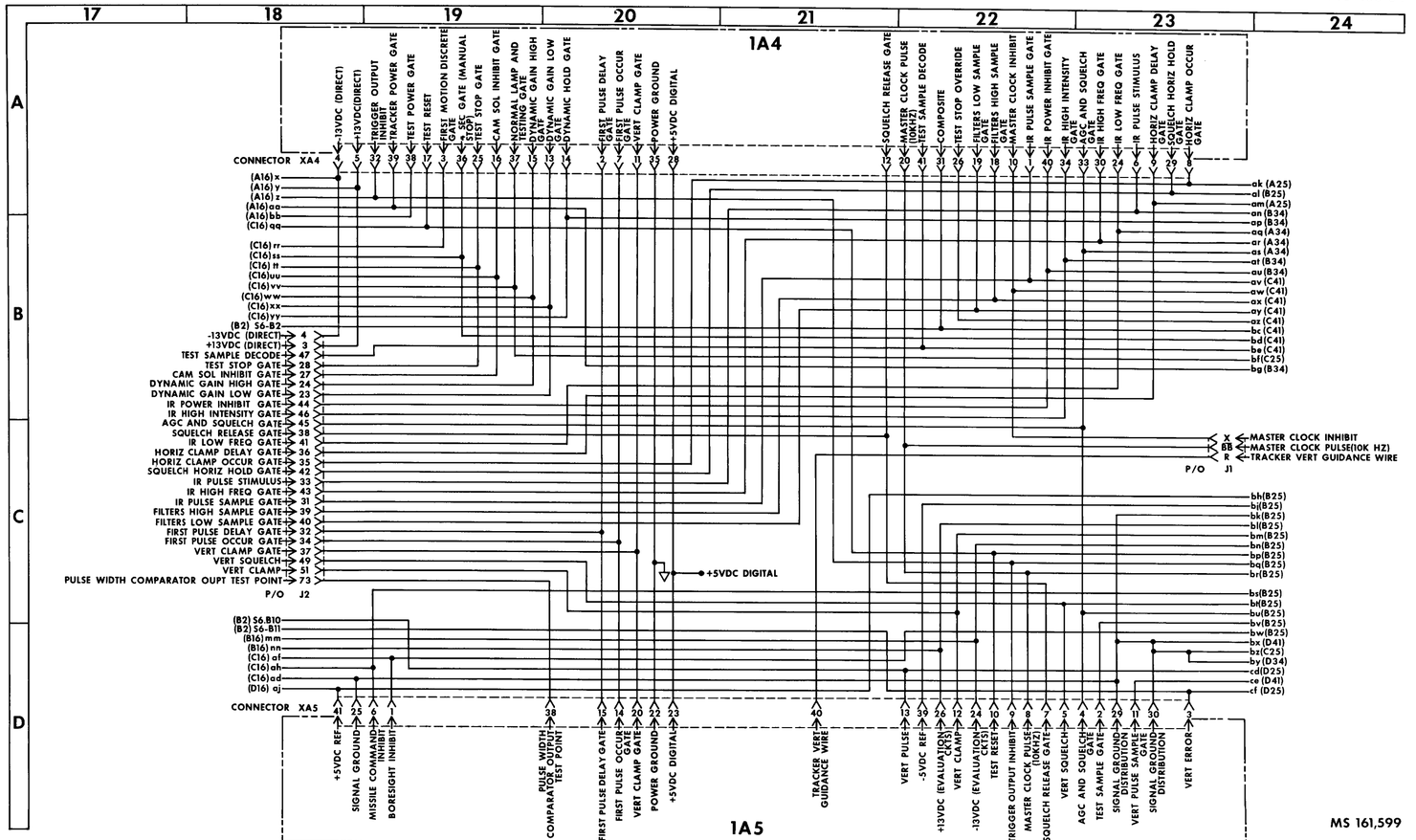

Figure 2-25. Monitor unit (10277941) - schematic diagram (sheet 3 of 6)

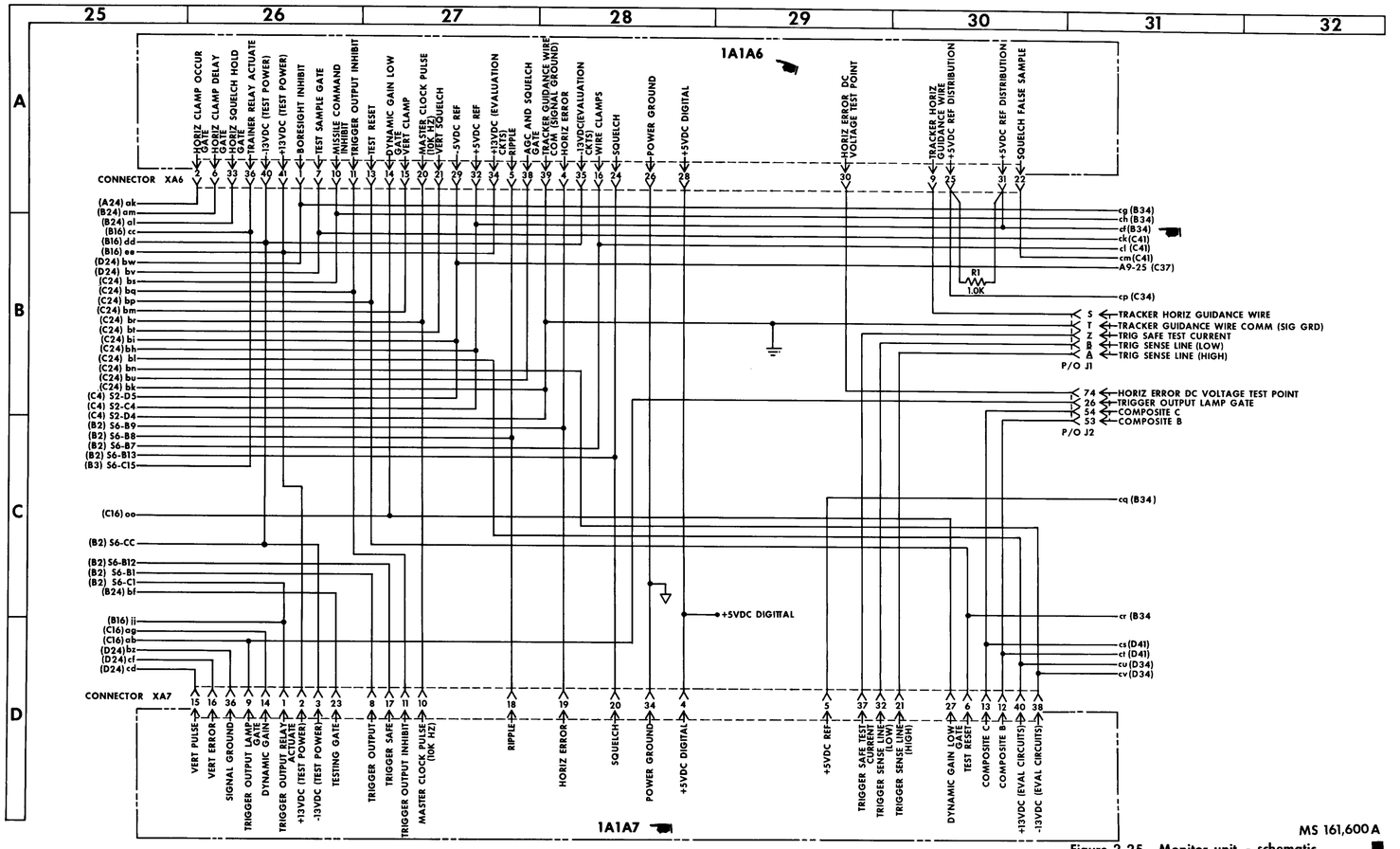

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Figure 2-25. Monitor unit - schematic diagram (sheet 4 of 6)

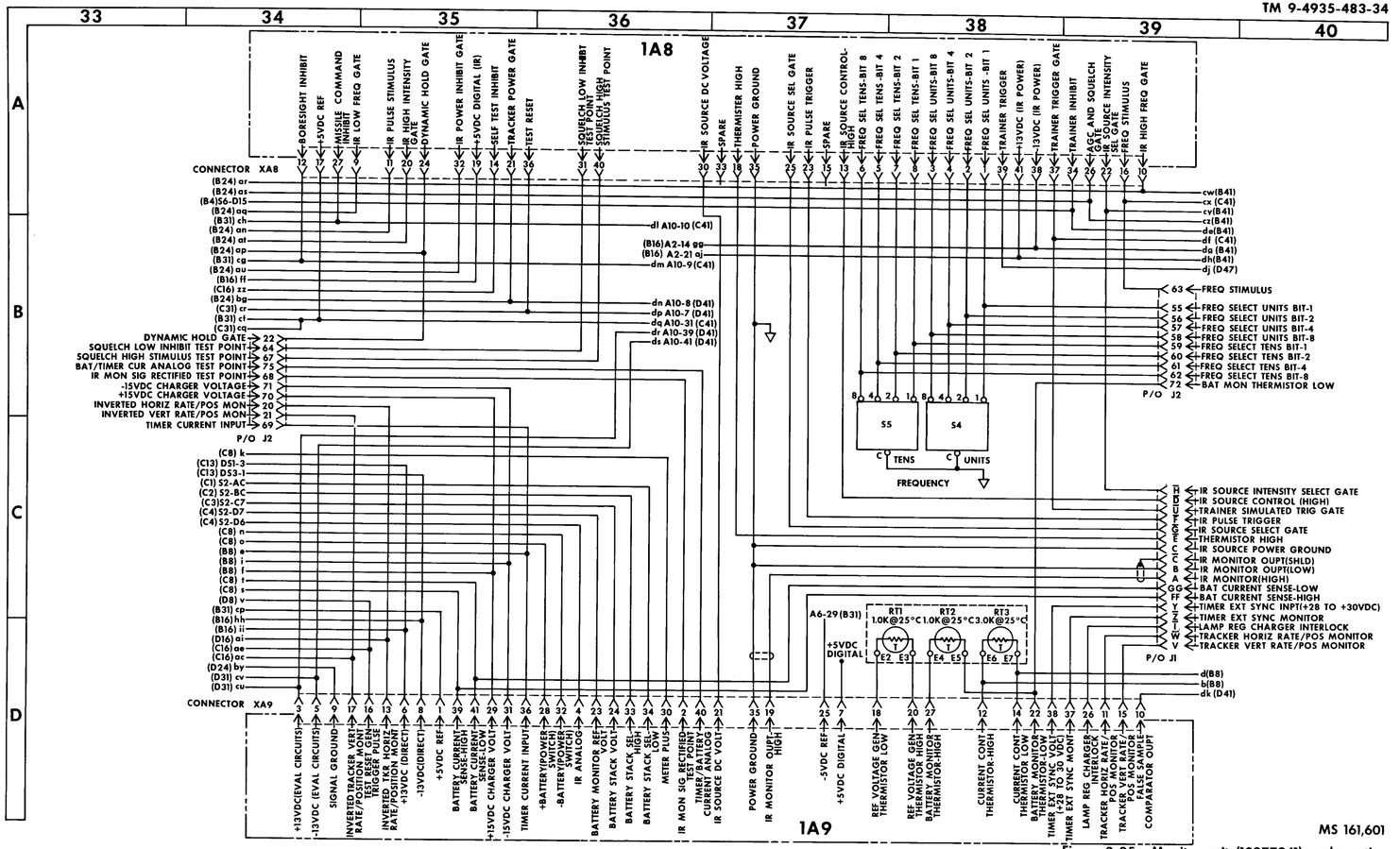

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Figure 2-25. Monitor unit (10277941) - schematic diagram (sheet 5 of 6)

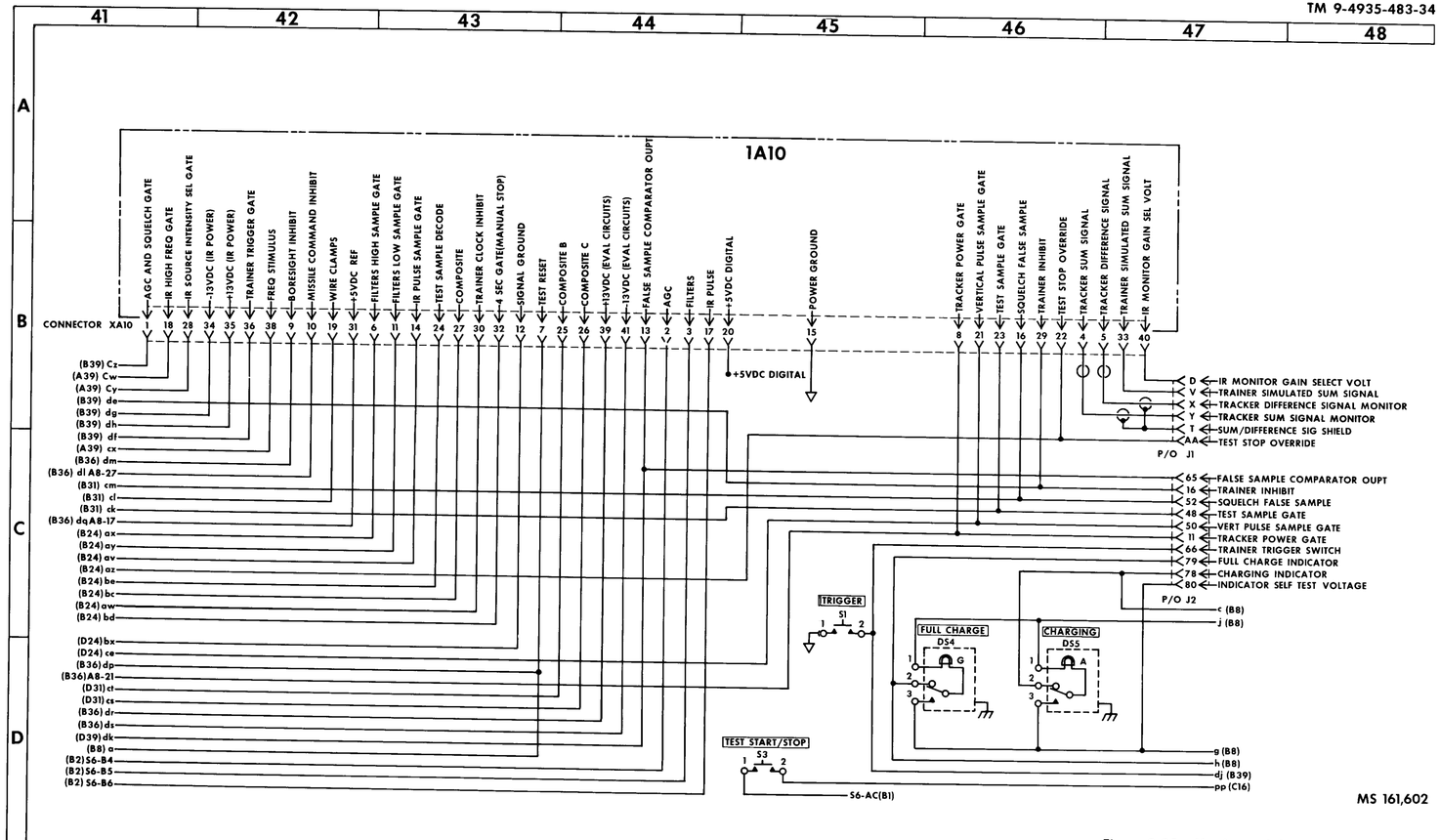

Figure 2-25. Monitor unit (10277941) - schematic diagram (sheet 6 of 6)

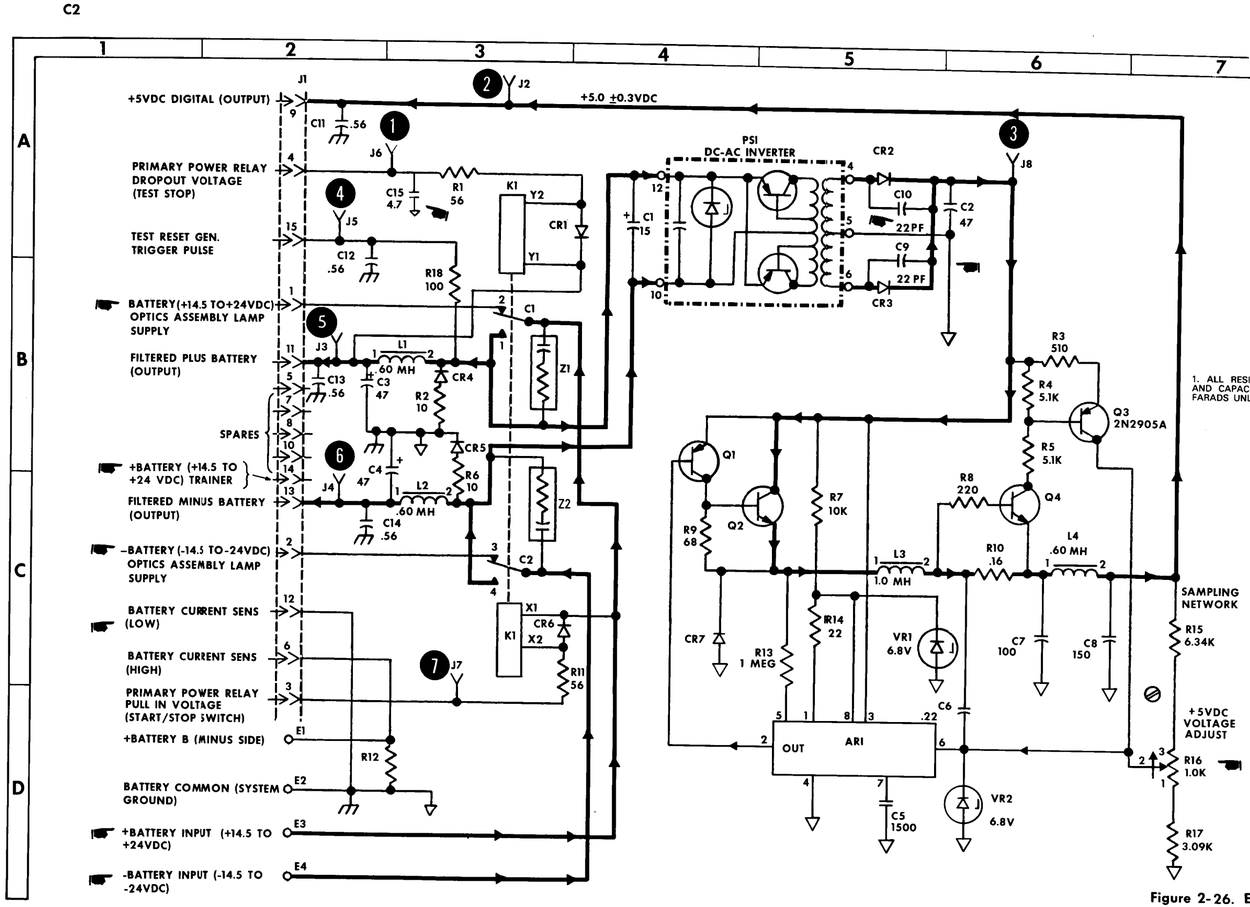

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Figure 2-26. Electronic components assembly 1A1A1 - schematic diagram (sheet 1 of 2)

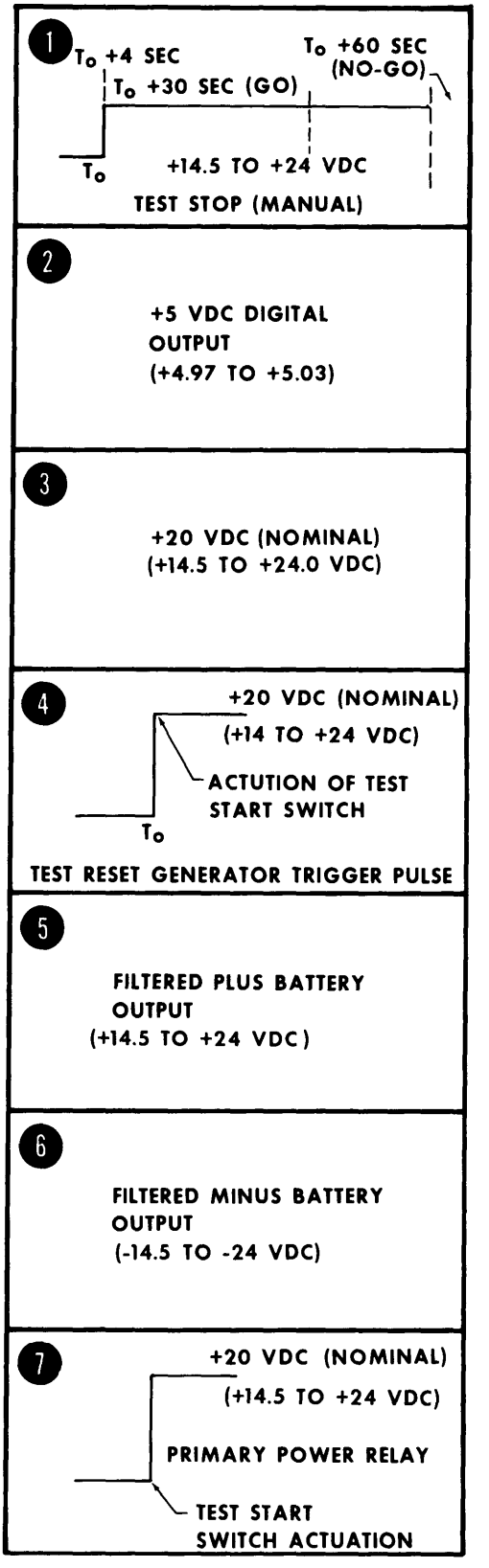

Figure 2-26. Electronic components assembly 1A1 (10219959) - schematic diagram (sheet 2 of 2)

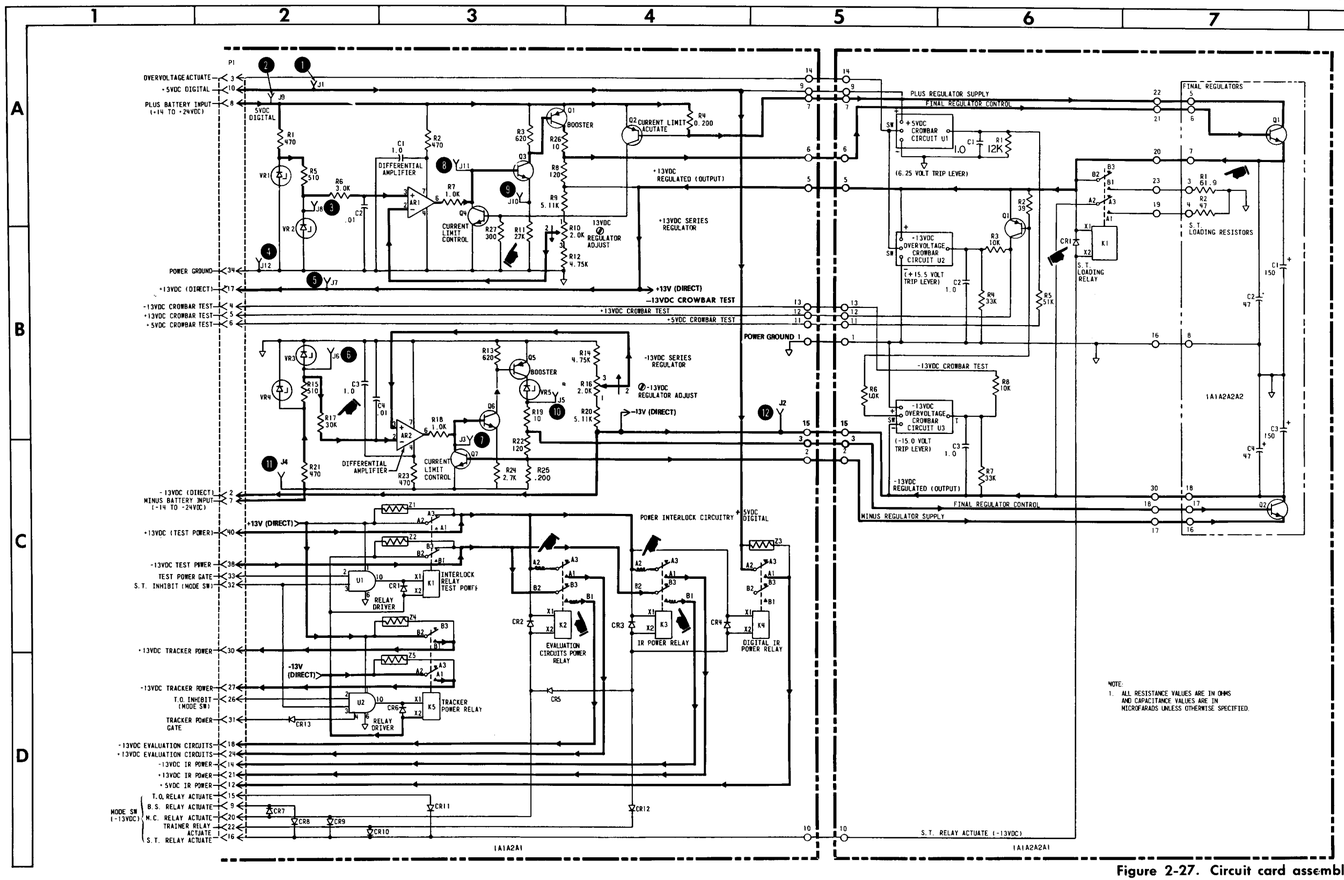

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Figure 2-27. Circuit card assembly 1A1A2 - schematic diagram (sheet 1 of 2)

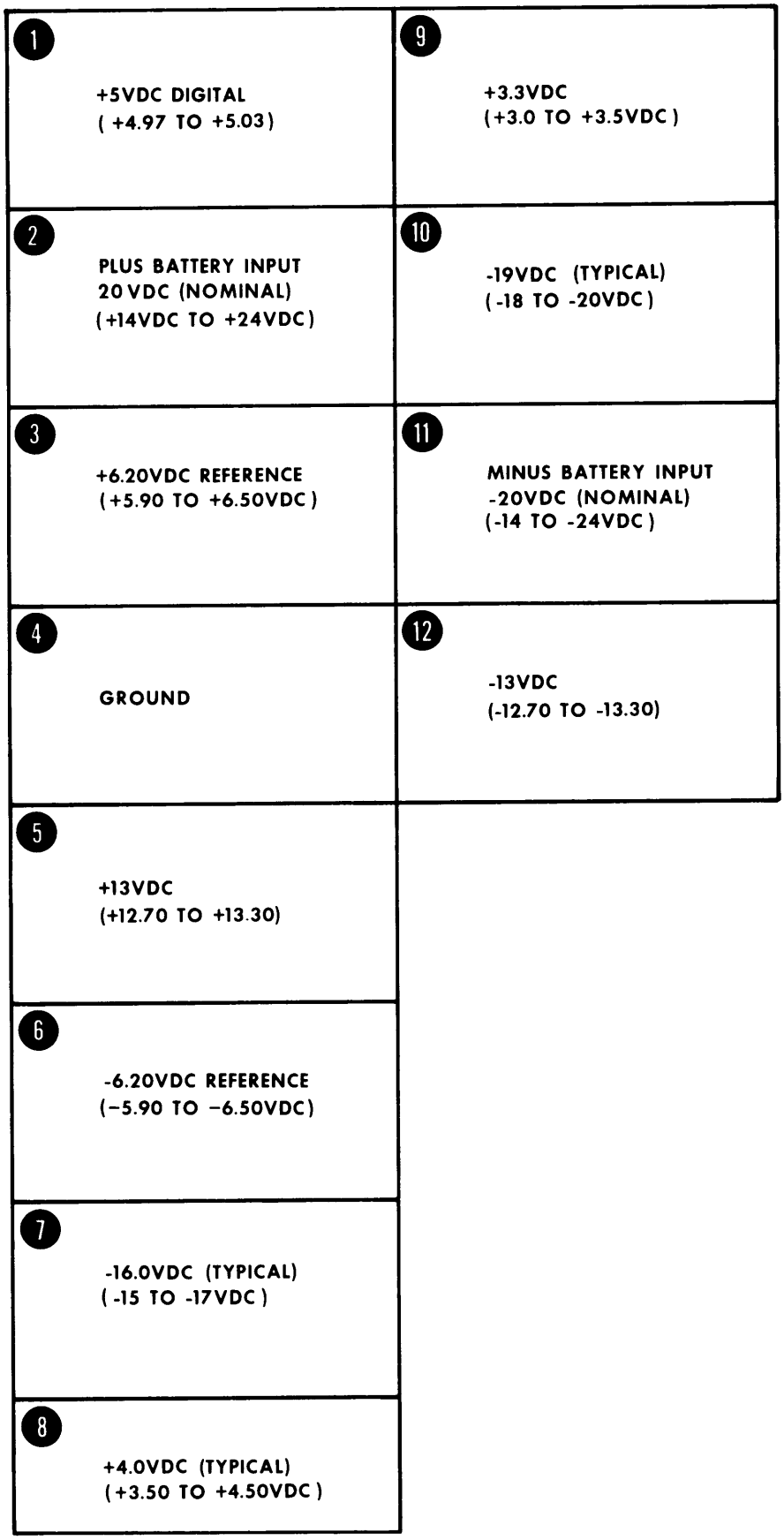

Figure 2-27. Circuit card assembly 1A2 - (10278351) schematic diagram (sheet 2 of 2)

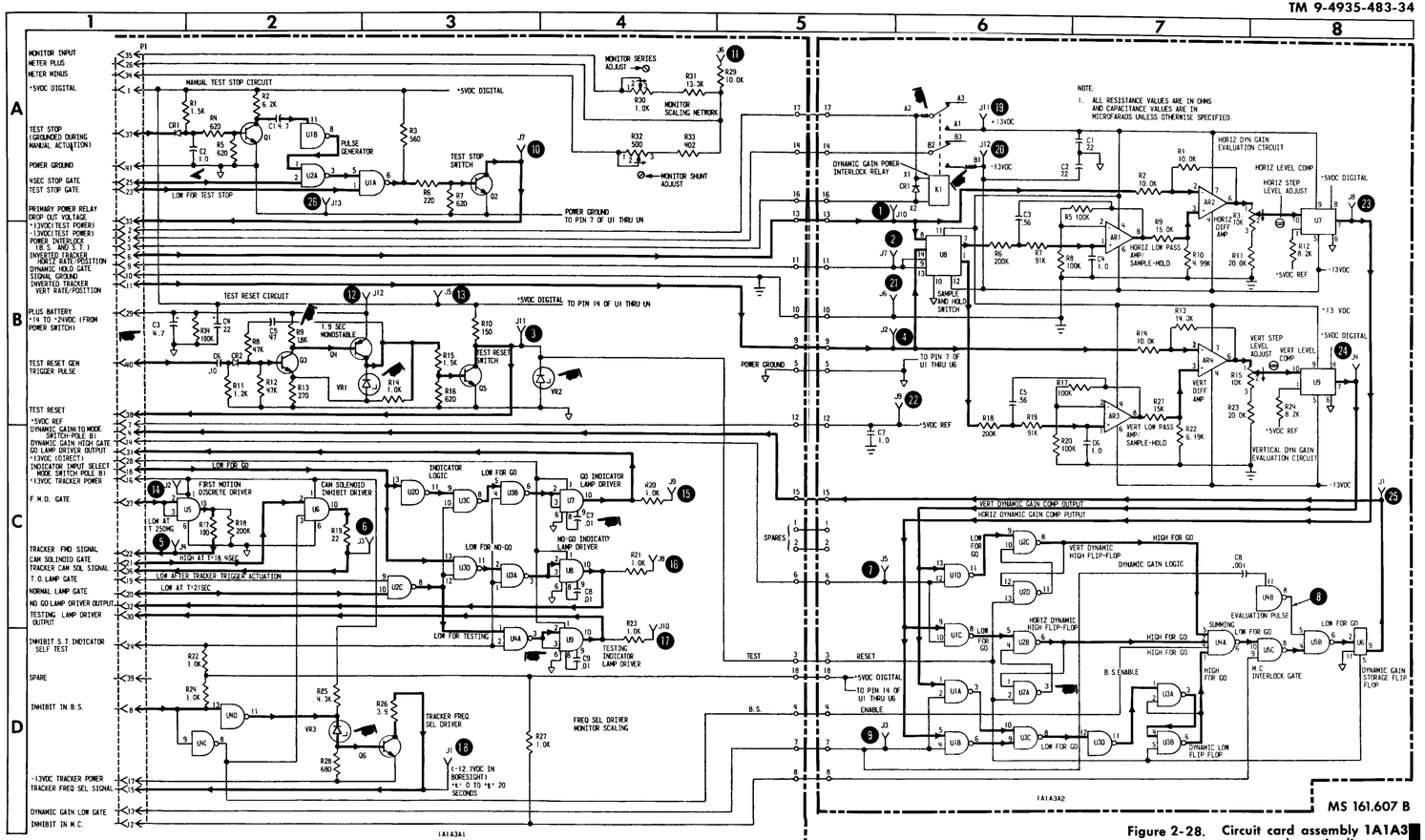

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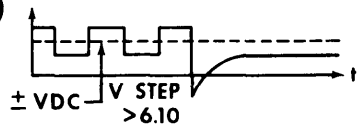
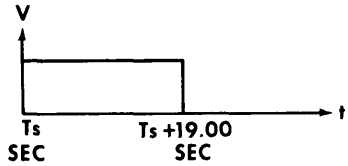
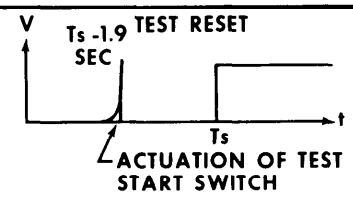
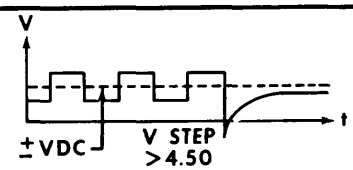
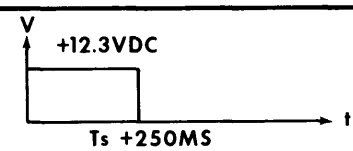
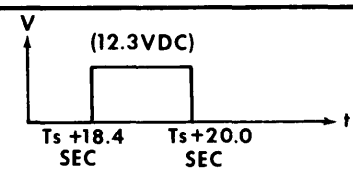
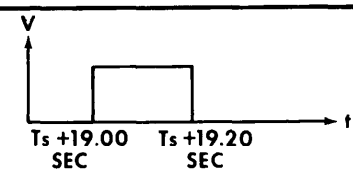
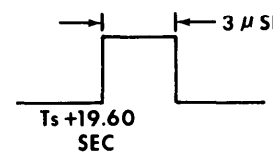
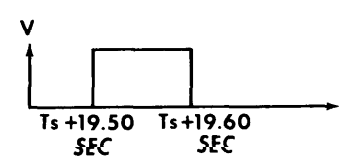
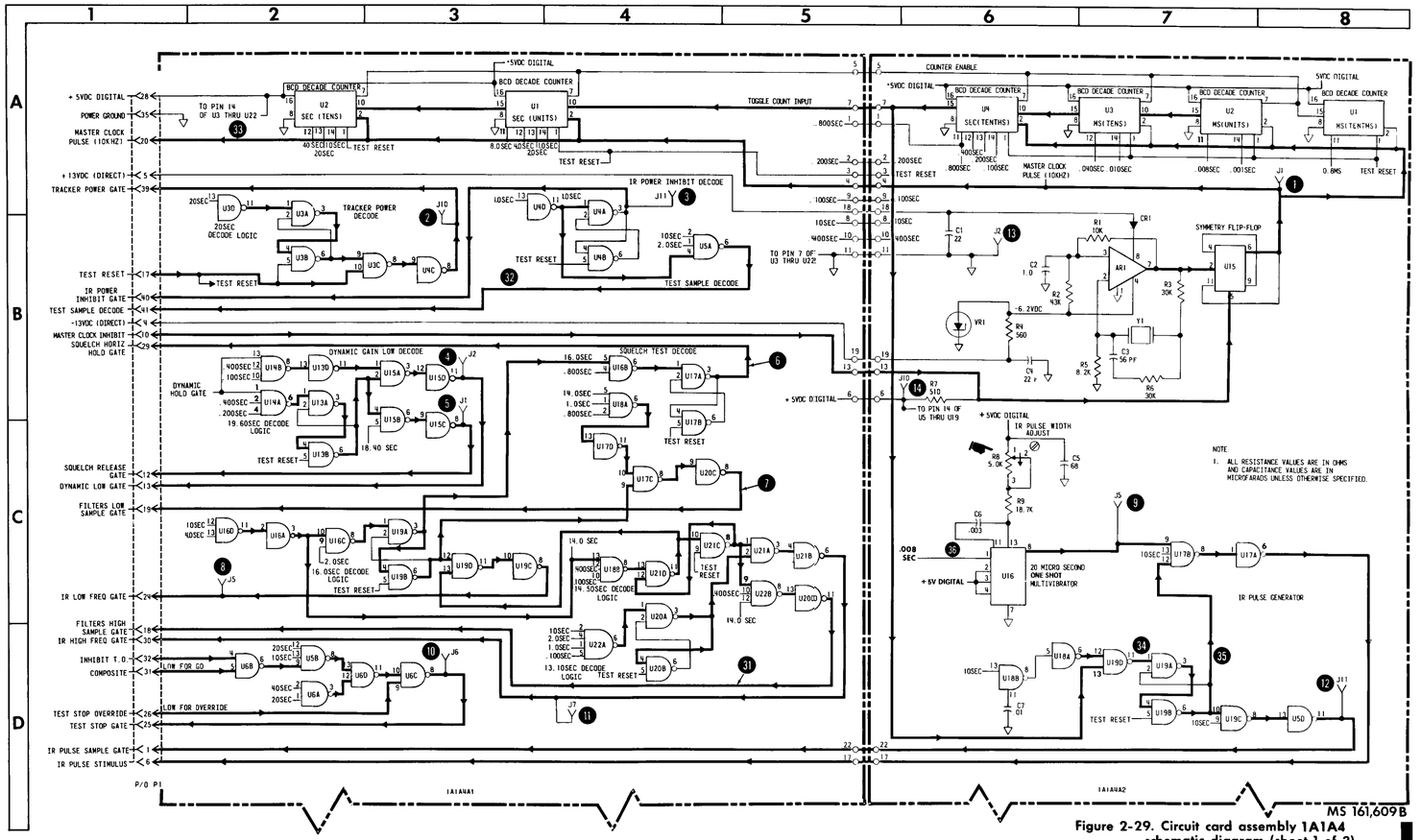
Figure 2-28. Circuit card assembly 1A1A3 schematic diagram (sheet 1 of 2)

1 	10 (+14 TO +24VDC) FOR TEST FROM Ts +1.9 SEC TO TEST STOP	19 -13.0VDC (+12.70 TO +13.30) Ts THROUGH Ts +21.0 SEC
2 	11 CALIBRATE VOLTAGE INPUT TO METER	20 -13.0 VDC (-12.70 TO -13.30) FROM Ts THROUGH Ts +21 SEC
3 	12 +14 TO +24VDC	21 SIGNAL GROUND
4 	13 +5VDC DIGITAL (4.97 TO 5.03)	22 +5VDC REFERENCE (+4.99 TO +5.01 VDC)
5 	14 +13 VDC IN BS AND MC FROM Ts THROUGH Ts +20	23 HORIZ DYNAMIC GAIN COMPARATOR OUTPUT (HIGH FOR GO)
6 	15 +12.3VDC FOR (GO) INDICATOR ON, FROM Ts +21 THROUGH Ts+30.0 SEC	24 VERT DYNAMIC GAIN COMPARATOR (HIGH FOR GO)
7 	16 +12.3VDC FOR (NO-GO) INDICATOR ON, FROM Ts +21 SEC THROUGH Ts +60 SEC	25 DYNAMIC GAIN (LOW FOR GO)
8 	17 +12.3VDC FOR (TESTING) INDICATOR ON, Ts THROUGH Ts+21 SEC	26 POWER GROUND
9 	18 -12.7VDC IN BS, Ts THROUGH Ts +20 SEC	

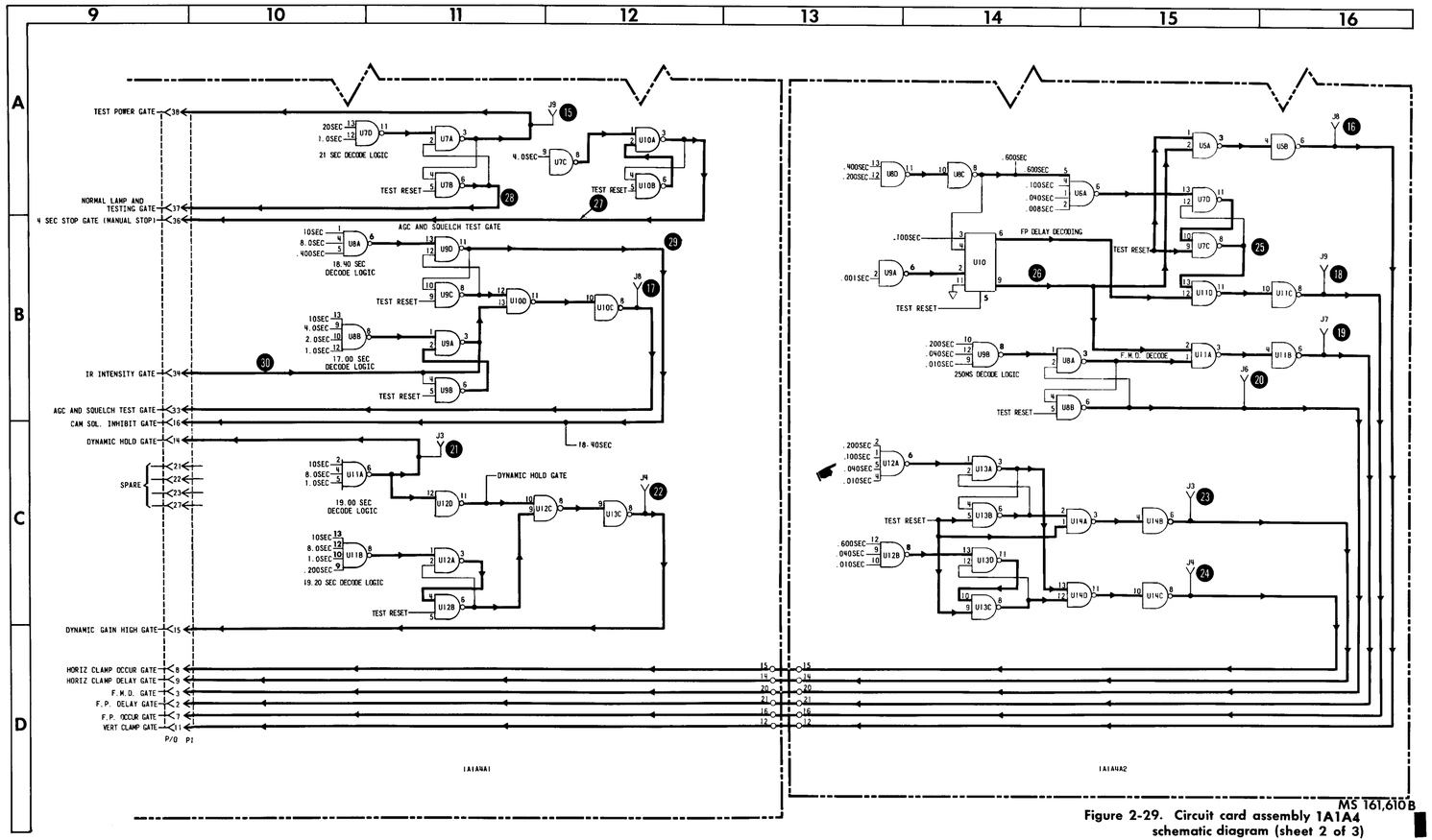
MS 161,608

Figure 2-28. Circuit card assembly 1A3 (10278354) - schematic diagram (sheet 2 of 2)



MS 161,609B

Figure 2-29. Circuit card assembly 1A1A4 schematic diagram (sheet 1 of 3)



MS 161,610B

Figure 2-29. Circuit card assembly 1A1A4 schematic diagram (sheet 2 of 3)

1 V, 0.1MS, t MASTER CLOCK PULSE	7 Ts +15.80 SEC, Ts +16.00 SEC FILTERS LOW SAMPLE GATE	13 POWER GROUND	19 Ts +250 MS, Ts +701 MS FIRST PULSE DELAY GATE	25 Ts +748 MS	31 Ts +14.40 SEC, Ts +14.50 SEC FILTERS HIGH SAMPLE GATE
2 Ts, Ts +20 SEC TRACKER POWER GATE	8 Ts +14.50 SEC, Ts +16.00 SEC IR LOW FREQ GATE	14 +5.0 ± 0.3 VDC DIGITAL (+4.70 TO +5.30)	20 TEST START AT Ts, Ts +250 MS FIRST MOTION DESCRETE GATE	26 Ts +701 MS	32 Ts +12.0 SEC, Ts +13.0 SEC TEST SAMPLE DECODE
3 Ts +1.0 SEC IR POWER INHIBIT GATE	9 V, W, t PULSE WIDTH(W)=20.0± 0.8US PRT=10.0 ± 0.1 MS IR PULSE STIMULUS	15 Ts +21 SEC TEST POWER GATE	21 Ts +19.00 SEC, Ts +20.00 SEC DYNAMIC HOLD GATE	27 Ts +4 SEC 4 SECOND STOP GATE	33 V, 0.1MS, t MASTER CLOCK PULSE (10KHz)
4 Ts +19.50 SEC, Ts +19.60 SEC DYNAMIC LOW GATE	10 Ts +30 SEC (GO) Ts +60 SEC (NO-GO) TEST STOP GATE	16 Ts, Ts +701 MS VERT CLAMP GATE	22 Ts +19.000 SEC, Ts +19.20 SEC DYNAMIC GAIN HIGH GATE	28 Ts +21 SEC NORMAL LAMP AND TESTING GATE	34 Ts +11 SEC LOW AT +11 SEC
5 Ts +18.40 SEC, Ts +19.60 SEC SQUELCH RELEASE GATE	11 Ts +13.10 SEC, Ts +14.50 SEC IR HIGH FREQ GATE	17 Ts +17.0 SEC, Ts +18.4 SEC AGC AND SQUELCH TEST GATE	23 Ts, Ts +350 MS HORIZ CLAMP DELAY GATE	29 Ts +18.4 SEC CAM SOLENOID INHIBIT GATE	35 Ts +11 SEC LOW AT Ts +11 SEC
6 Ts +16.80 SEC SQUELCH HORIZ HOLD GATE	12 Ts +10 SEC, Ts +11 SEC IR PULSE SAMPLE GATE	18 Ts +701 MS, Ts +748 MS FIRST PULSE OCCUR GATE	24 Ts +350 MS, Ts +650 MS HORIZ CLAMP OCCUR GATE	30 Ts +17 SEC IR INTENSITY GATE	36 2MS, 8MS, 10MS

MS 161,611

Figure 2-29. Circuit card assembly 1A4 - (10277931) schematic diagram (sheet 3 of 3)

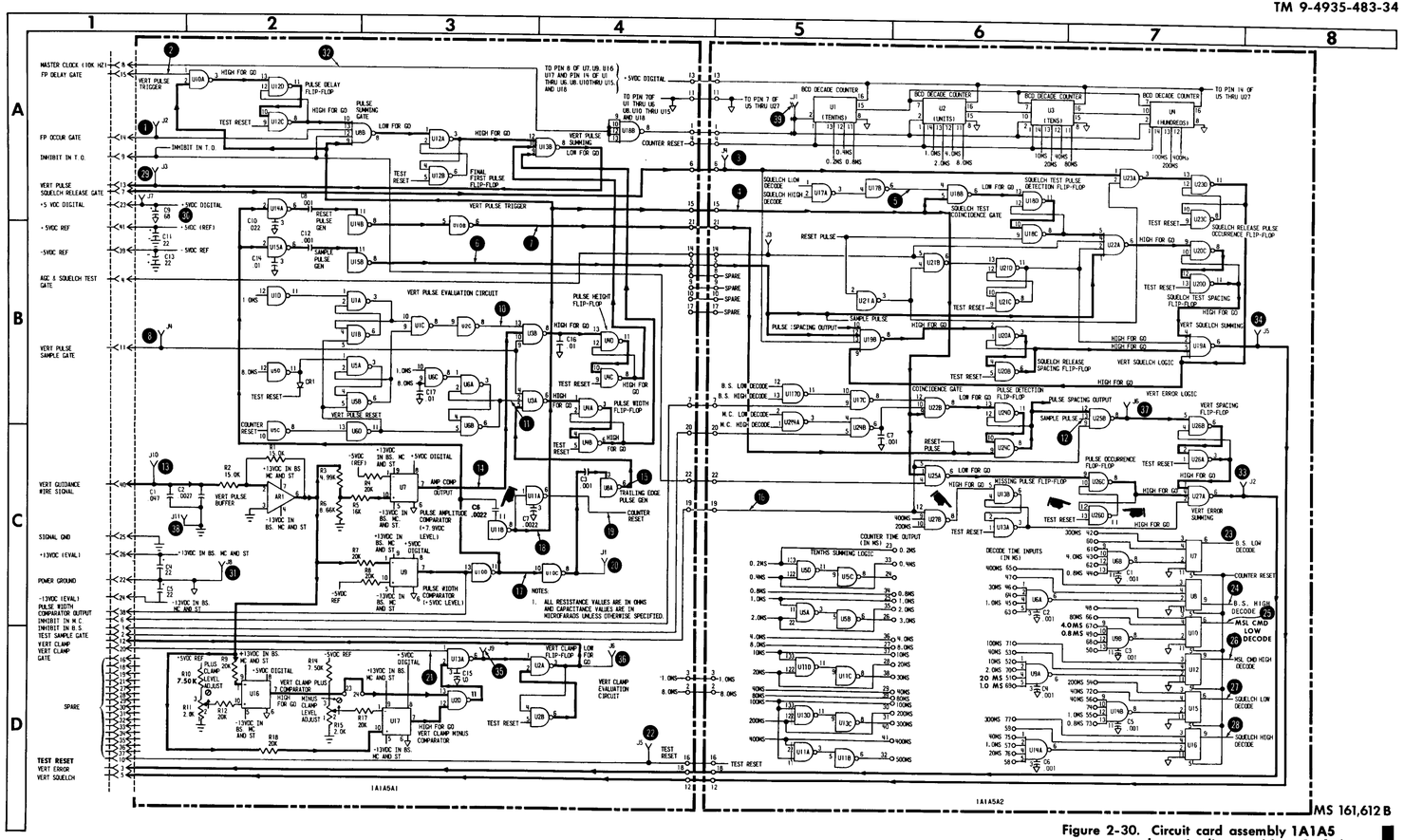
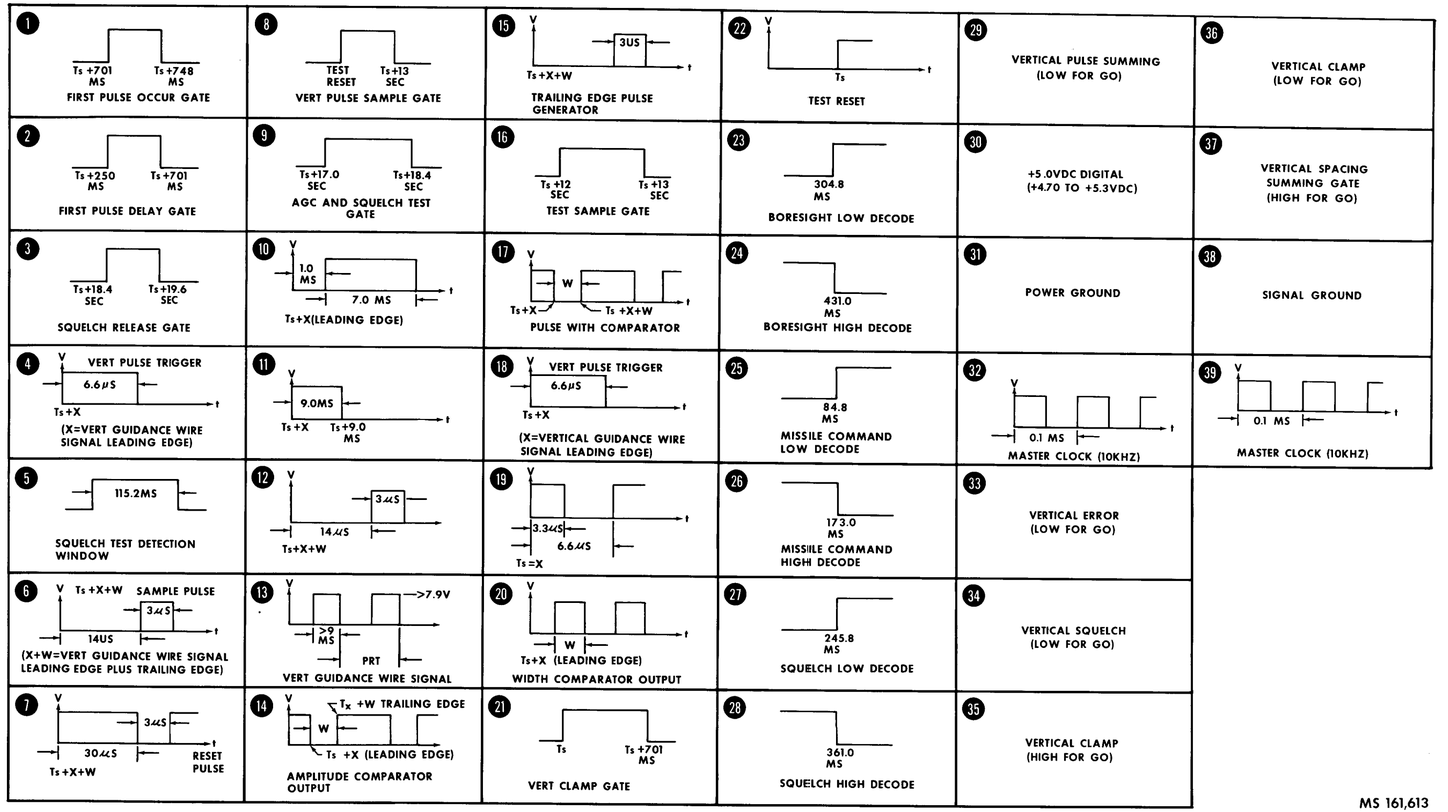
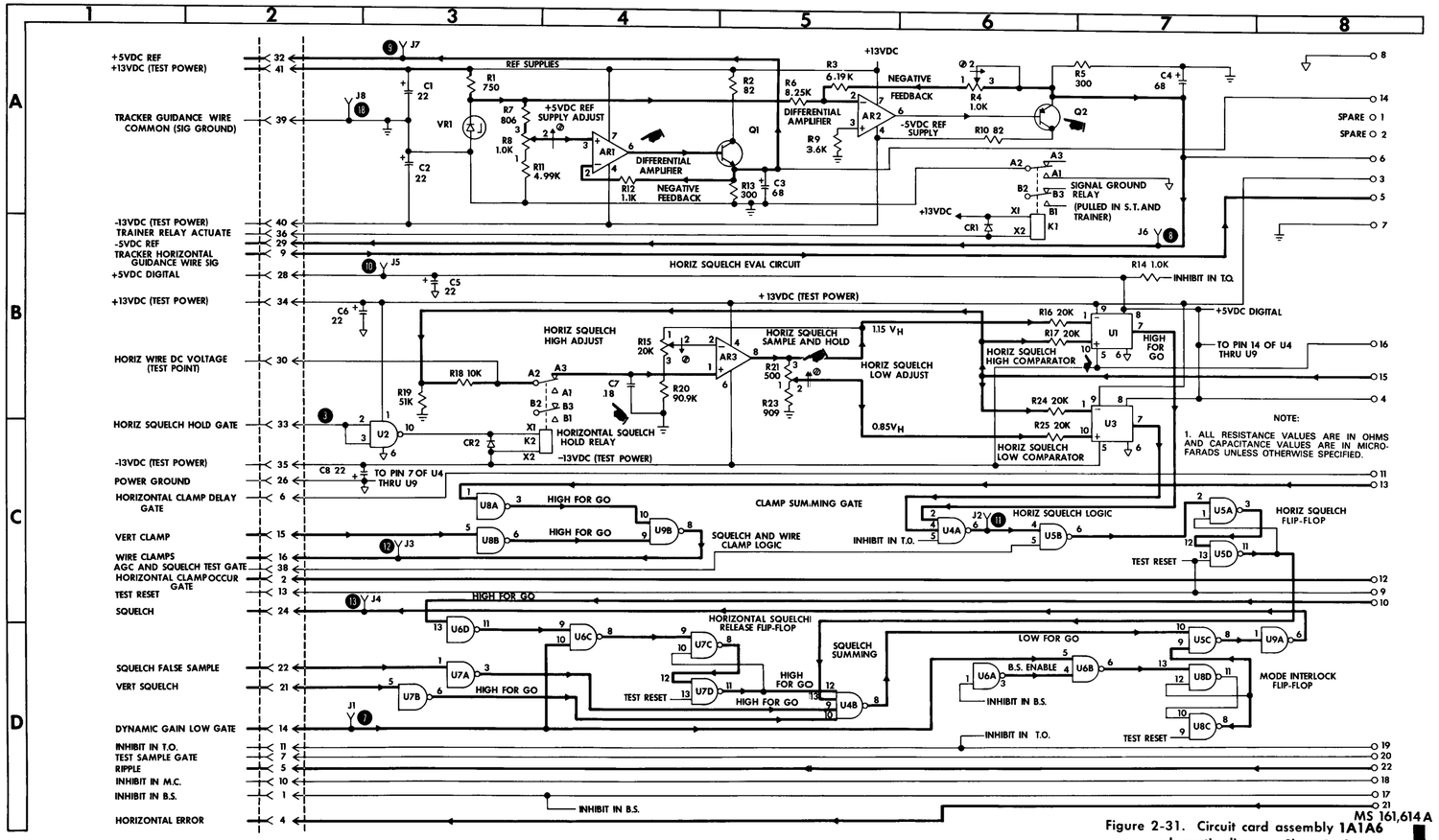


Figure 2-30. Circuit card assembly 1A1A5 - schematic diagram (sheet 1 of 2)



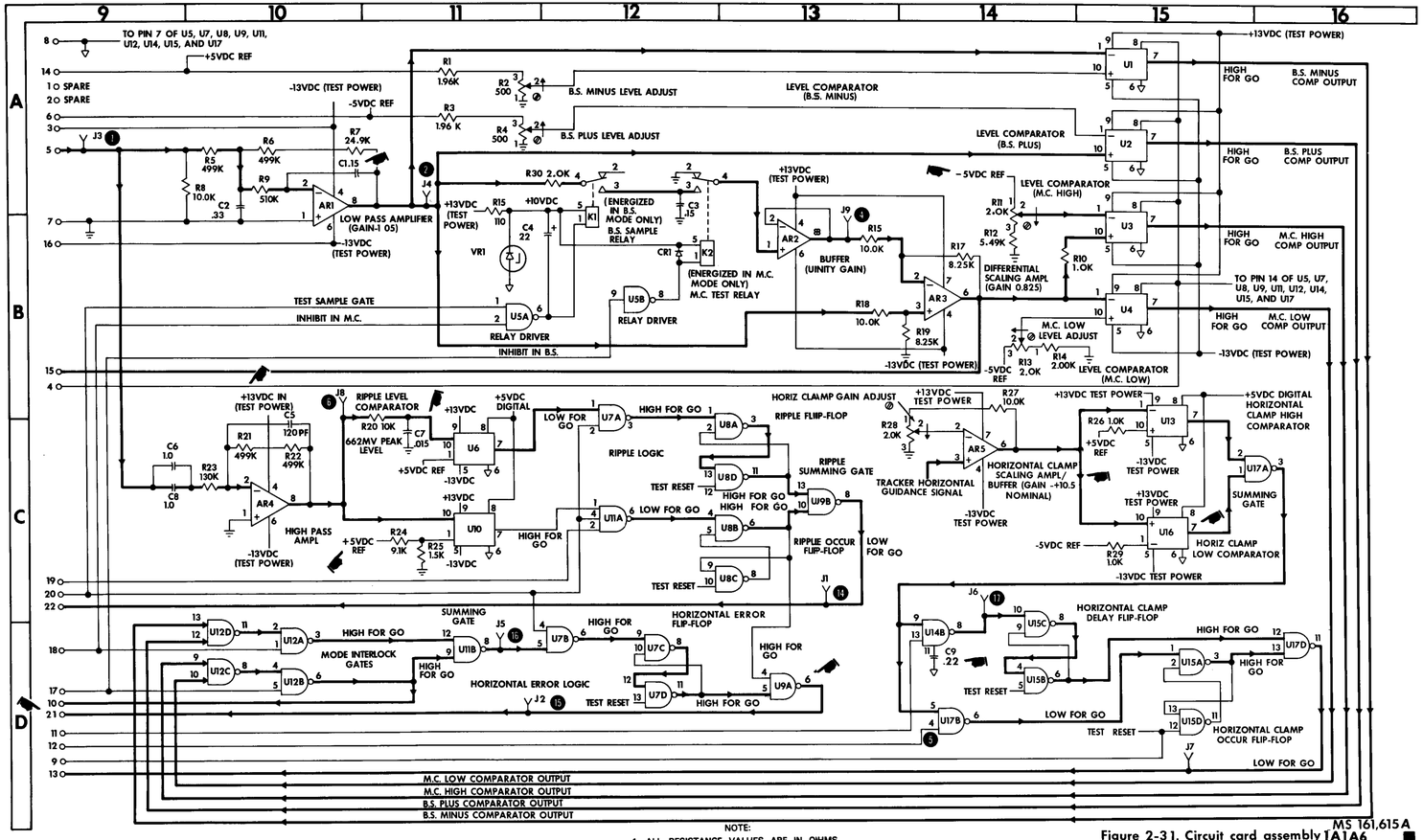
MS 161,613

Figure 2-30. Circuit card assembly 1A5 -(10277934) schematic diagram (sheet 2 of 2)



MS 161,614A

Figure 2-31. Circuit card assembly **1A1A6** - schematic diagram Sheet 1 of 3

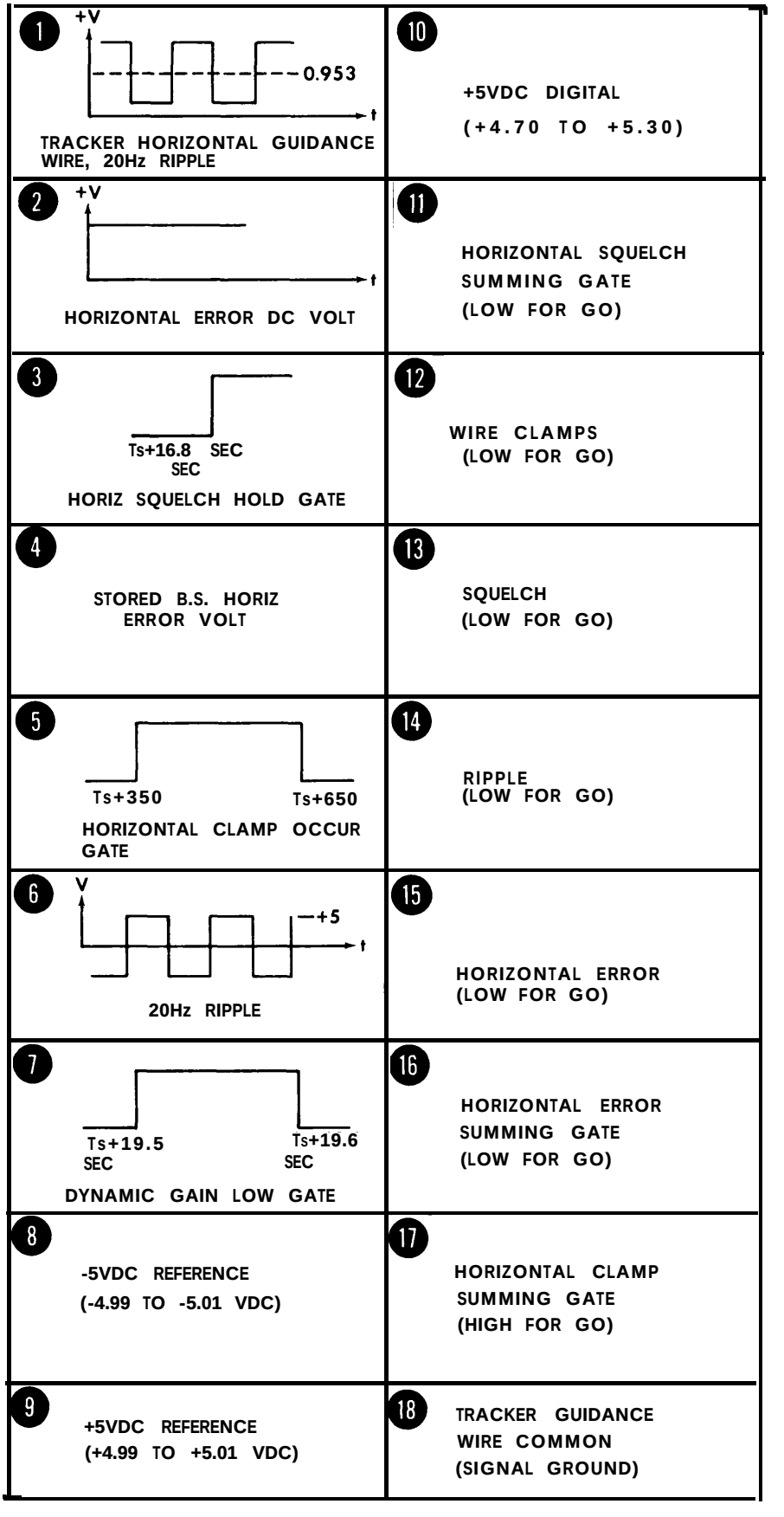


NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICRO-FARADS UNLESS OTHERWISE SPECIFIED.

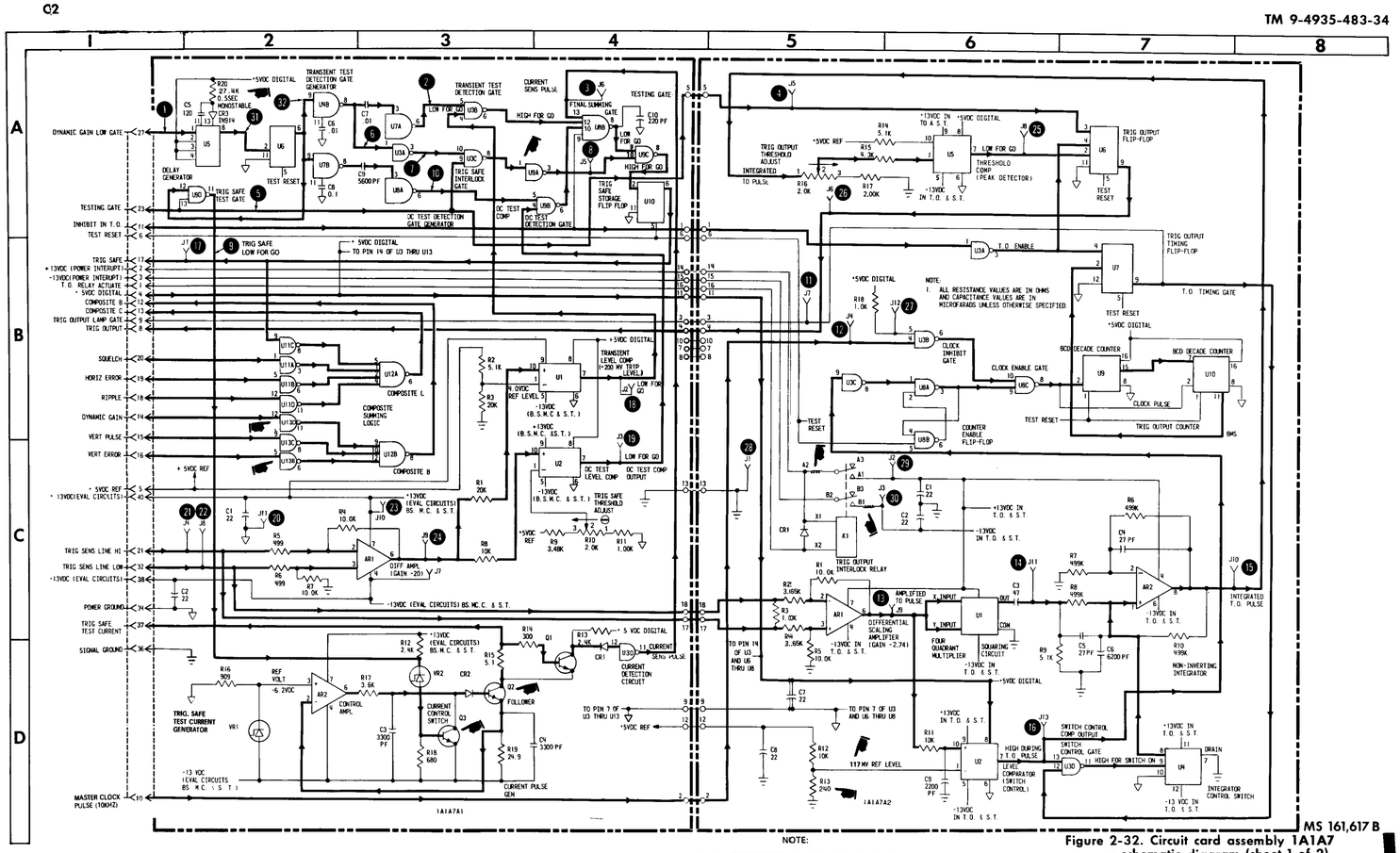
MS 161,615A

Figure 2-31. Circuit card assembly 1A1A6 schematic diagram Sheet 2 of 3



MS 161,616

Figure 2-31. Circuit card assembly 1A6 (10277929) - schematic diagram (sheet 3 of 3)



NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

MS 161,617 B

Figure 2-32. Circuit card assembly 1A1A7 - schematic diagram (sheet 1 of 2)

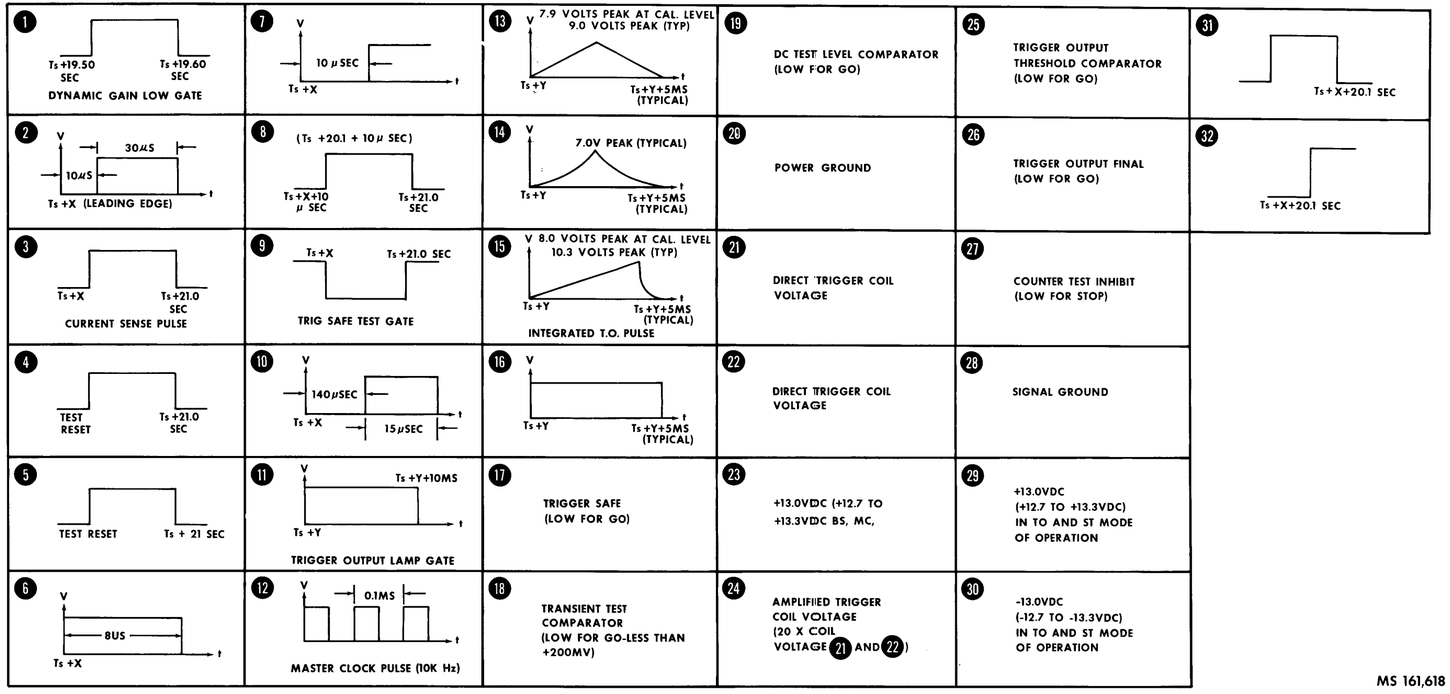
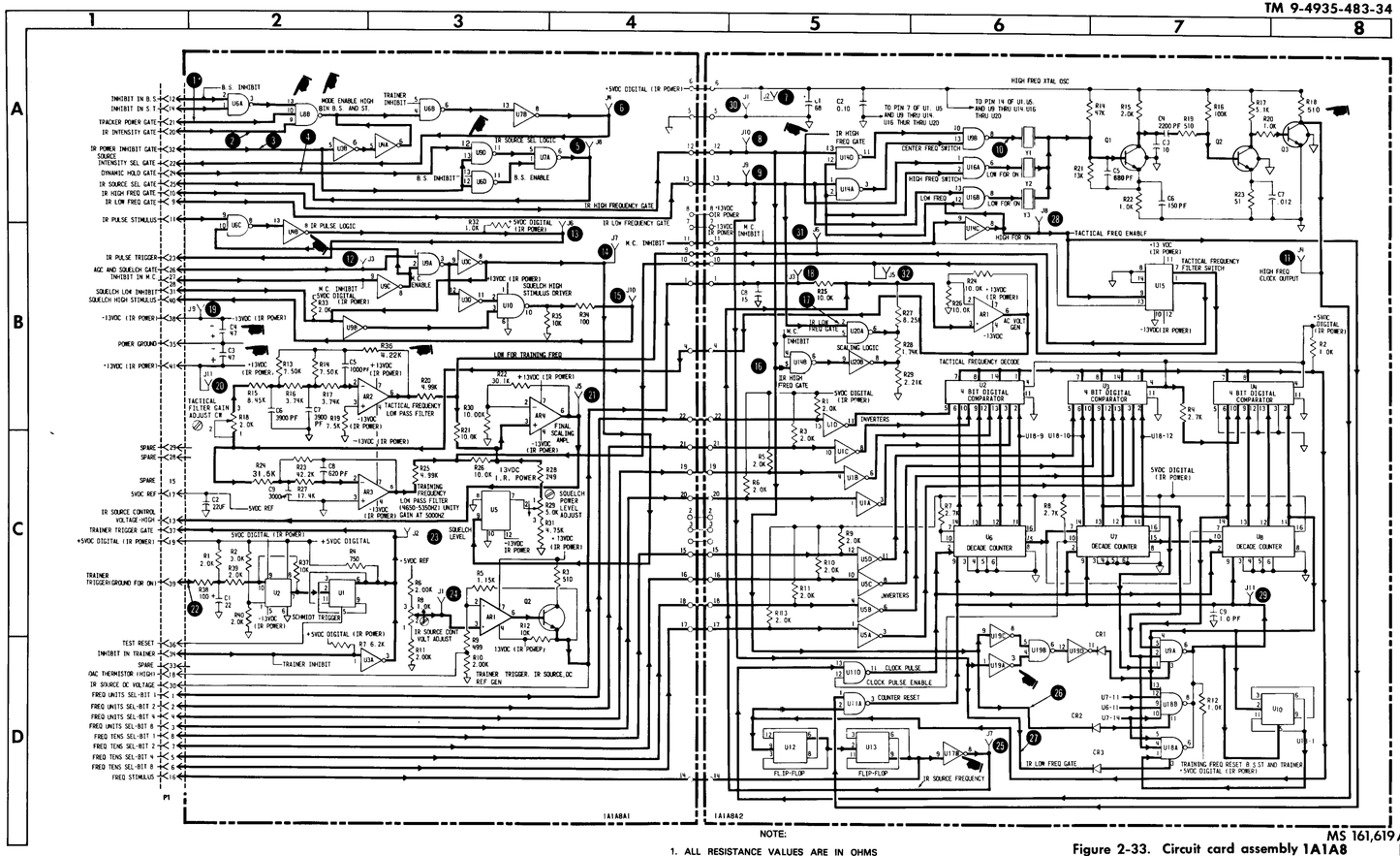


Figure 2-32. Circuit card assembly 1A7 (10277935)-schematic diagram (sheet 2 of 2)

C2

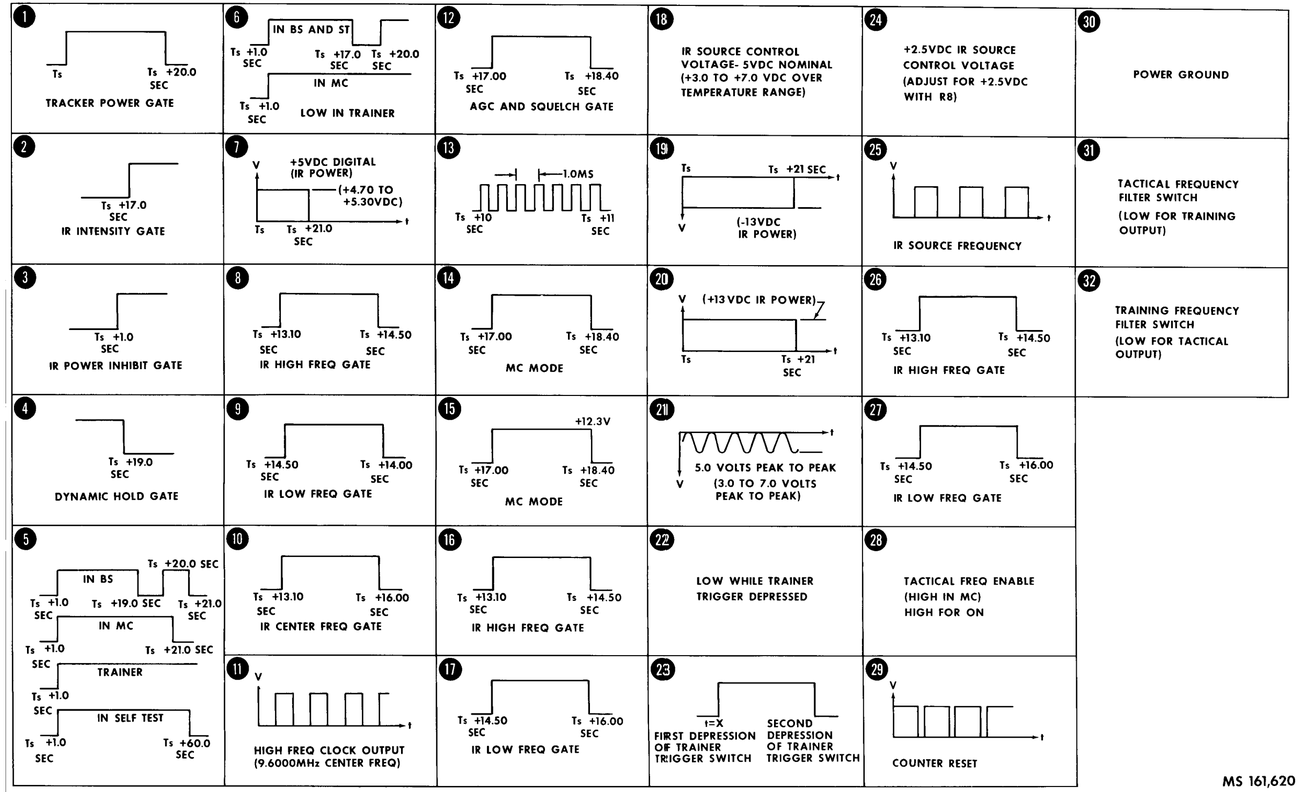


NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

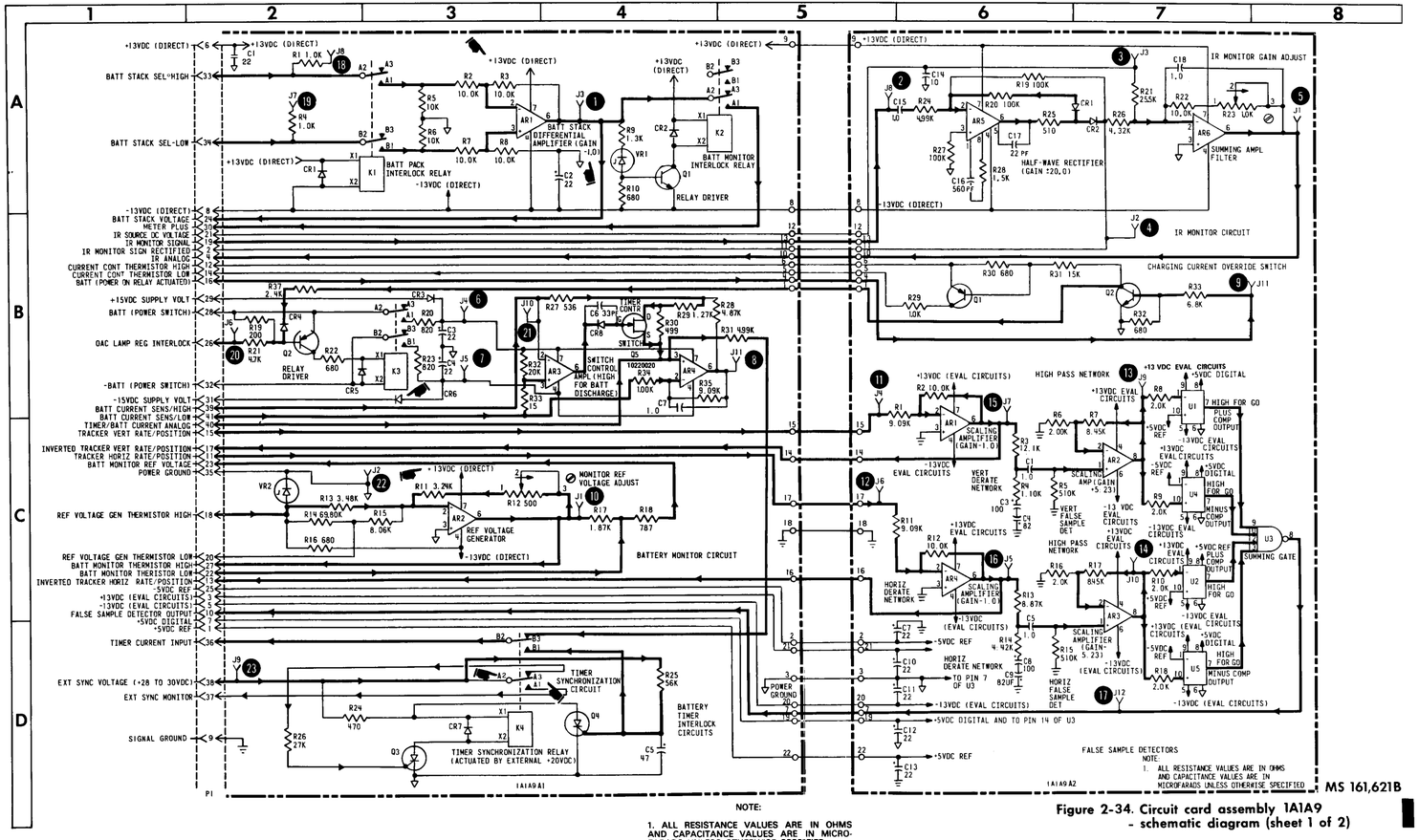
MS 161,619A

Figure 2-33. Circuit card assembly 1A1A8 - schematic diagram (sheet 1 of 2)



MS 161,620

Figure 2-33. Circuit card assembly 1A8 (10278379) - schematic diagram (sheet 2 of 2)

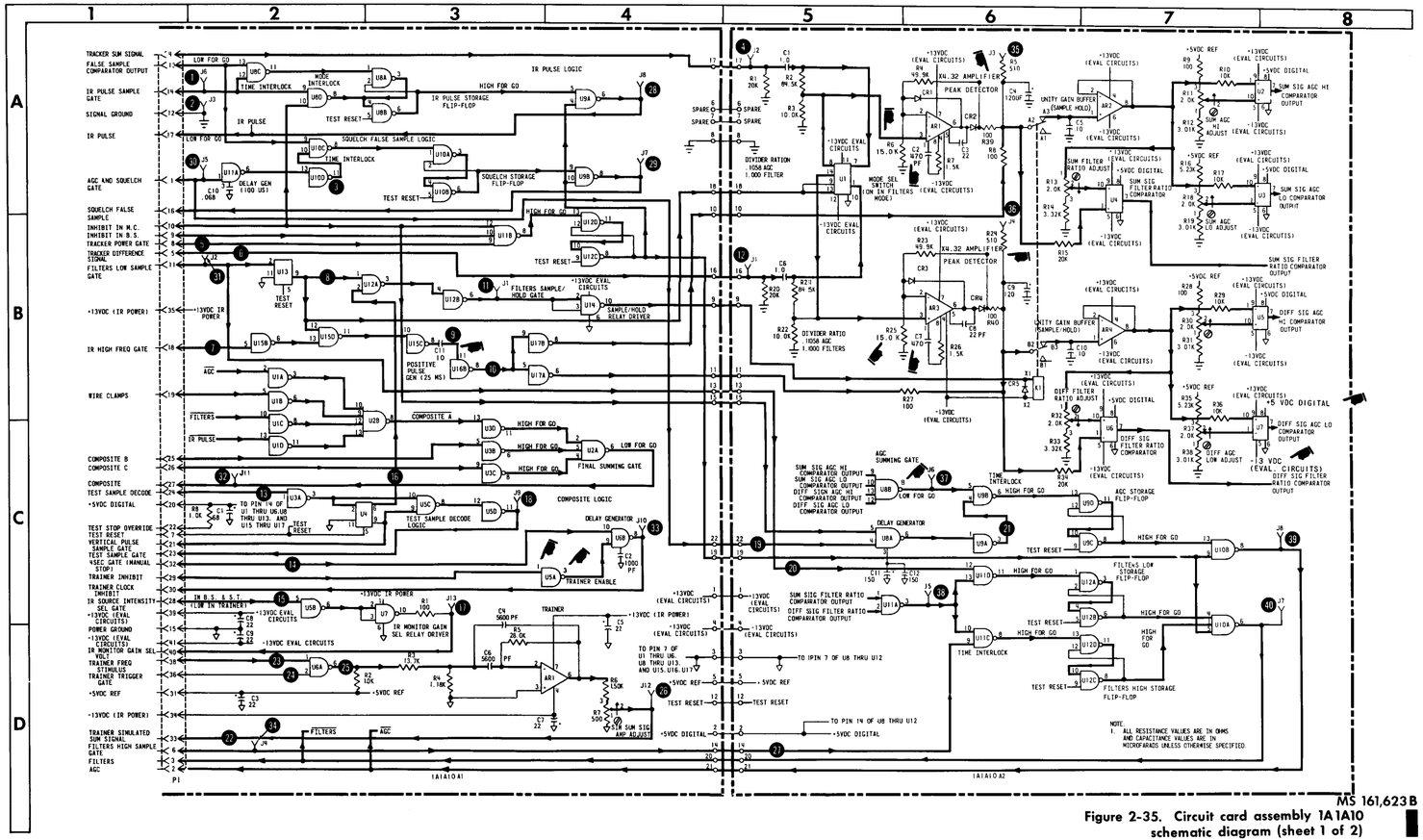


NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

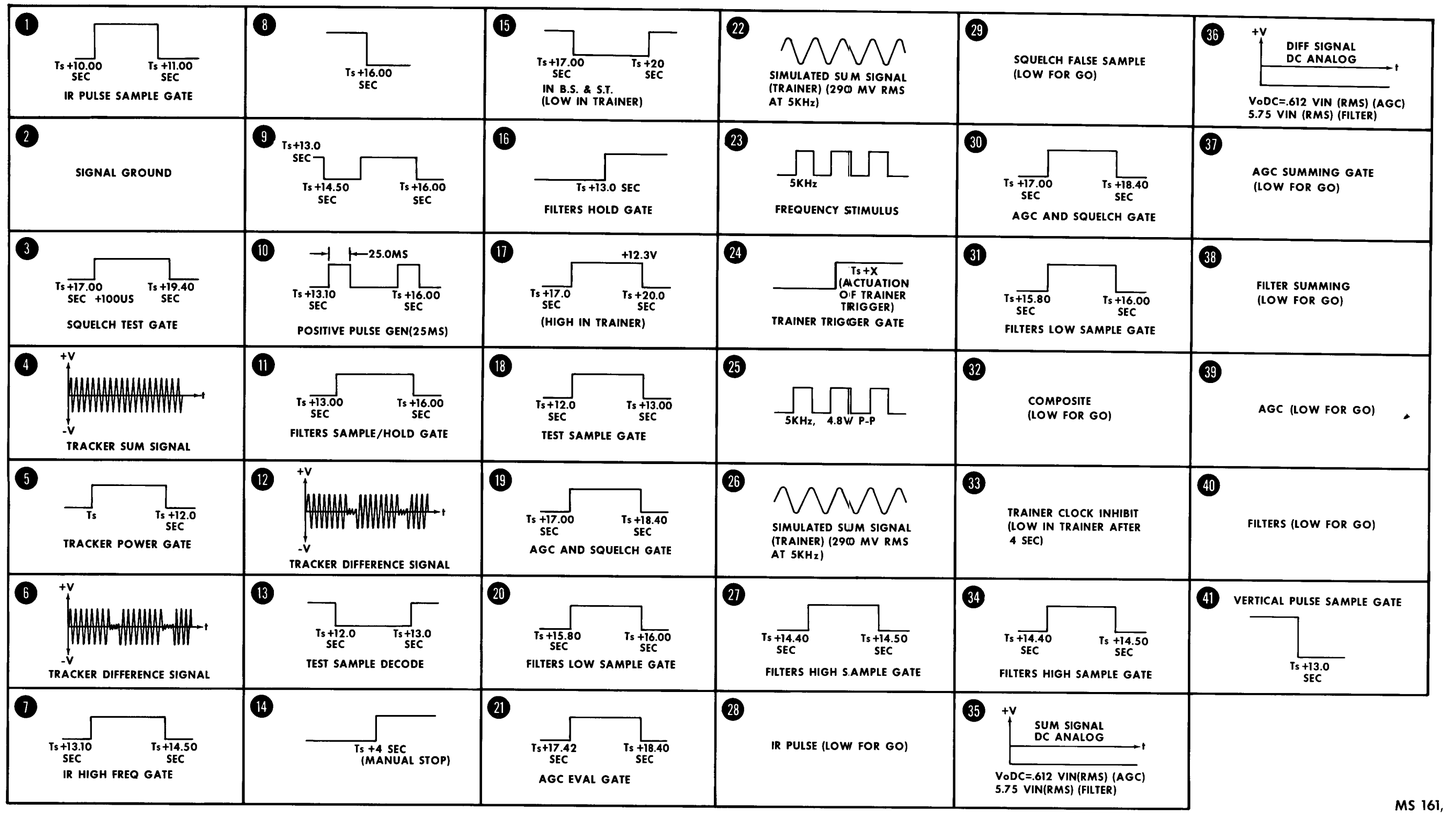
MS 161,621B

Figure 2-34. Circuit card assembly 1A1A9 - schematic diagram (sheet 1 of 2)



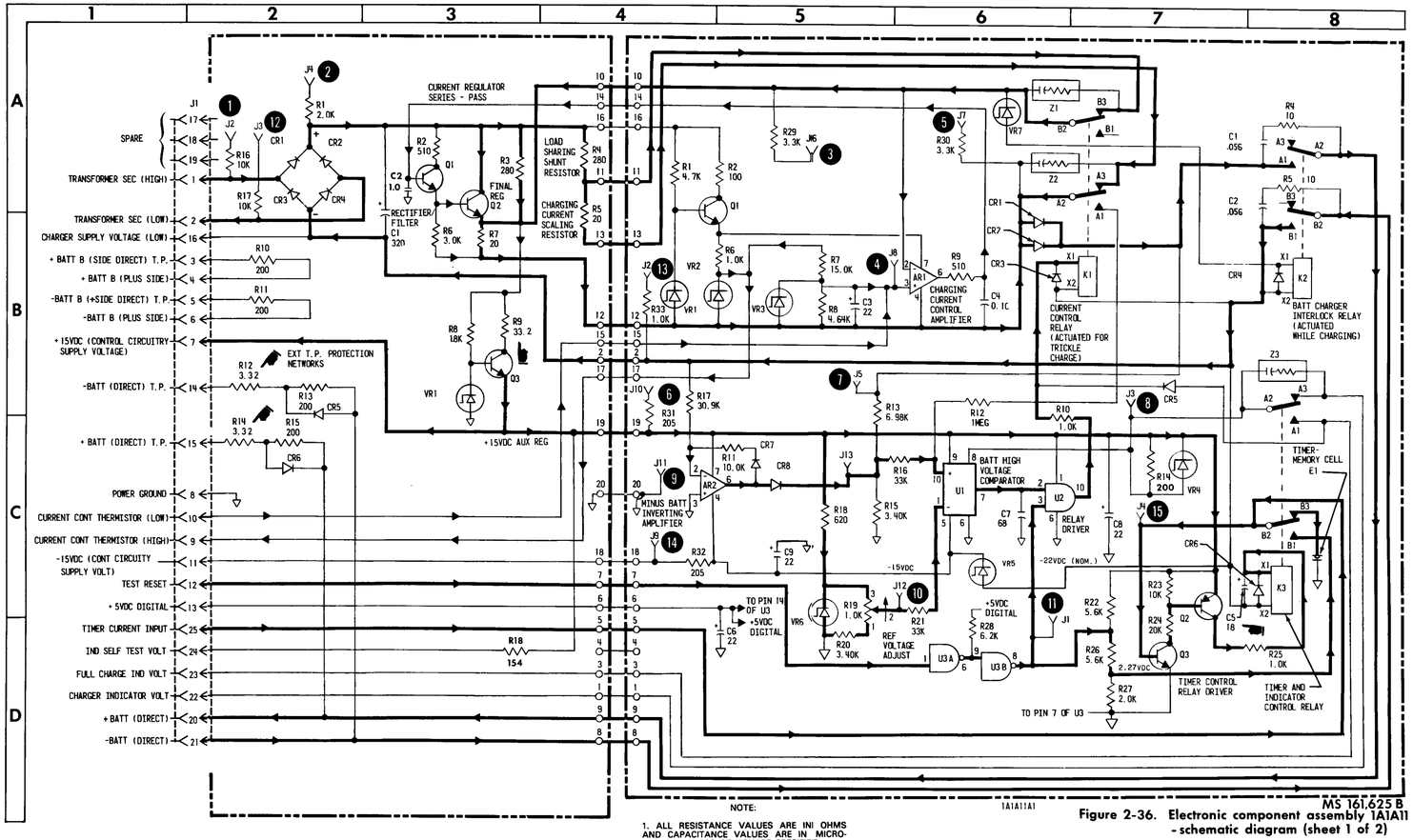
MS 161,623B

Figure 2-35. Circuit card assembly 1A1A10 schematic diagram (sheet 1 of 2)



MS 161,624

Figure 2-35. Circuit card assembly 1A10 (10278326)-schematic diagram (sheet 2 of 2)



NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

1A1A11A1

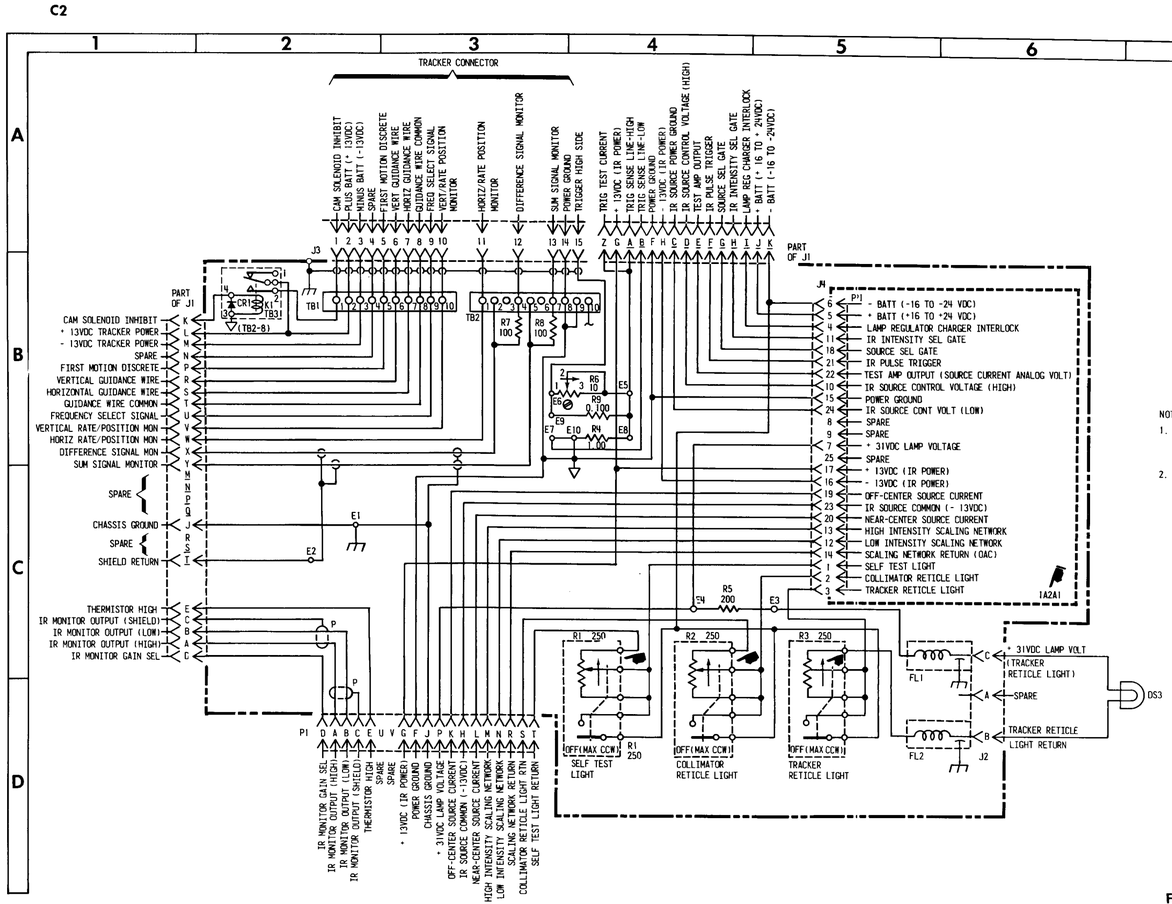
MS 161.625 B

Figure 2-36. Electronic component assembly 1A1A11 - schematic diagram (sheet 1 of 2)

1 65VAC NOMINAL (55 TO 75 VAC @ 50 TO 440 Hz)	8 +5.00VDC (+4.97 TO +5.03) CHARGER INDICATOR SUPPLY VOLTAGE	15 +3MVDC TYPICAL WHILE CHARGING
2 +75VDC NOMINAL (+60 TO +90VDC 10 VOLTS AC PEAK TO PEAK RIPPLE)	9 POWER GROUND	
3 +29VDC TYPICAL (+25 TO +30VDC) CONTROL AMPLIFIER FEEDBACK VOLTAGE	10 +8.20 VDC (AJD FOR +8.20VDC) VOLTAGE REFERENCE, HIGH	
4 +6.OVDC TYPICAL (+2,0 TO 6.2VDC) CHARGING CURRENT REFERENCE VOLTAGE	11 +7.5VDC  Ts-1.9 SEC Ts SEC CHARGER RESET	
5 +23.5VDC (+22 TO 22.5VDC) CURRENT REGULATOR LOW	12 65VAC NOMINAL (55 TO 75 VAC @ 50 TO 440 HZ)	
6 +15VDC (+13 TO +17VDC)	13 -22.5VDC (-21.5 TO -24.5VDC)	
7 22.5VDC (+22.5 TO +24.5VDC) + BATTERY CHARGER ON	14 -15VDC (-13 TO -17VDC)	

MS 161,626 A

Figure 2-36. Electronic component assembly 1A1A11 - schematic diagram (sheet 2 of 2)



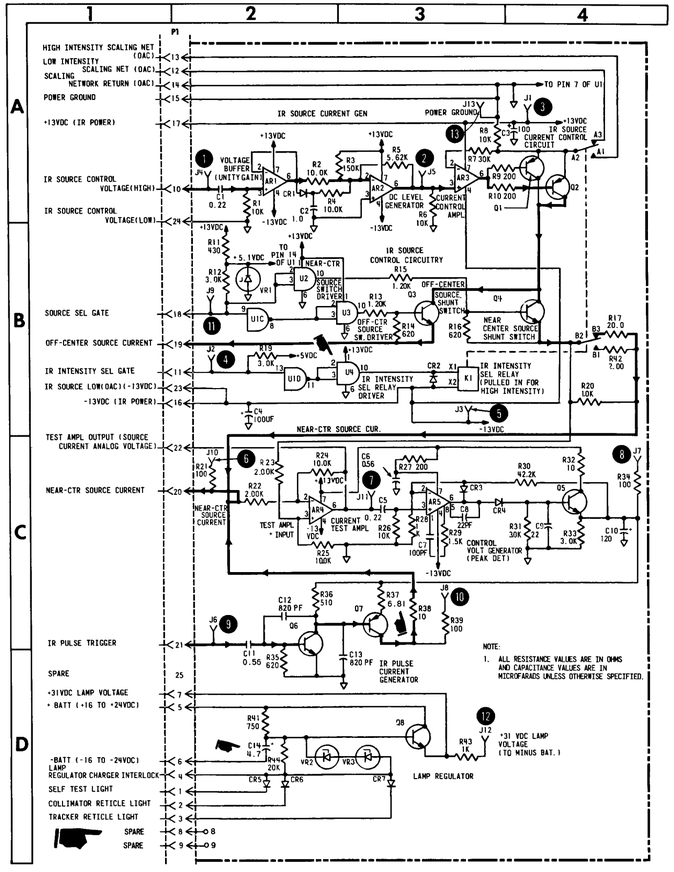
NOTES:

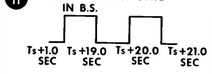
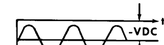
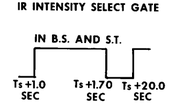
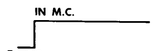
1. UNDERLINED LETTERS INDICATE LOWER CASE LETTERS.

2. ALL RESISTANCE VALUES IN OHMS AND CAPACITANCE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

MS 161,627A

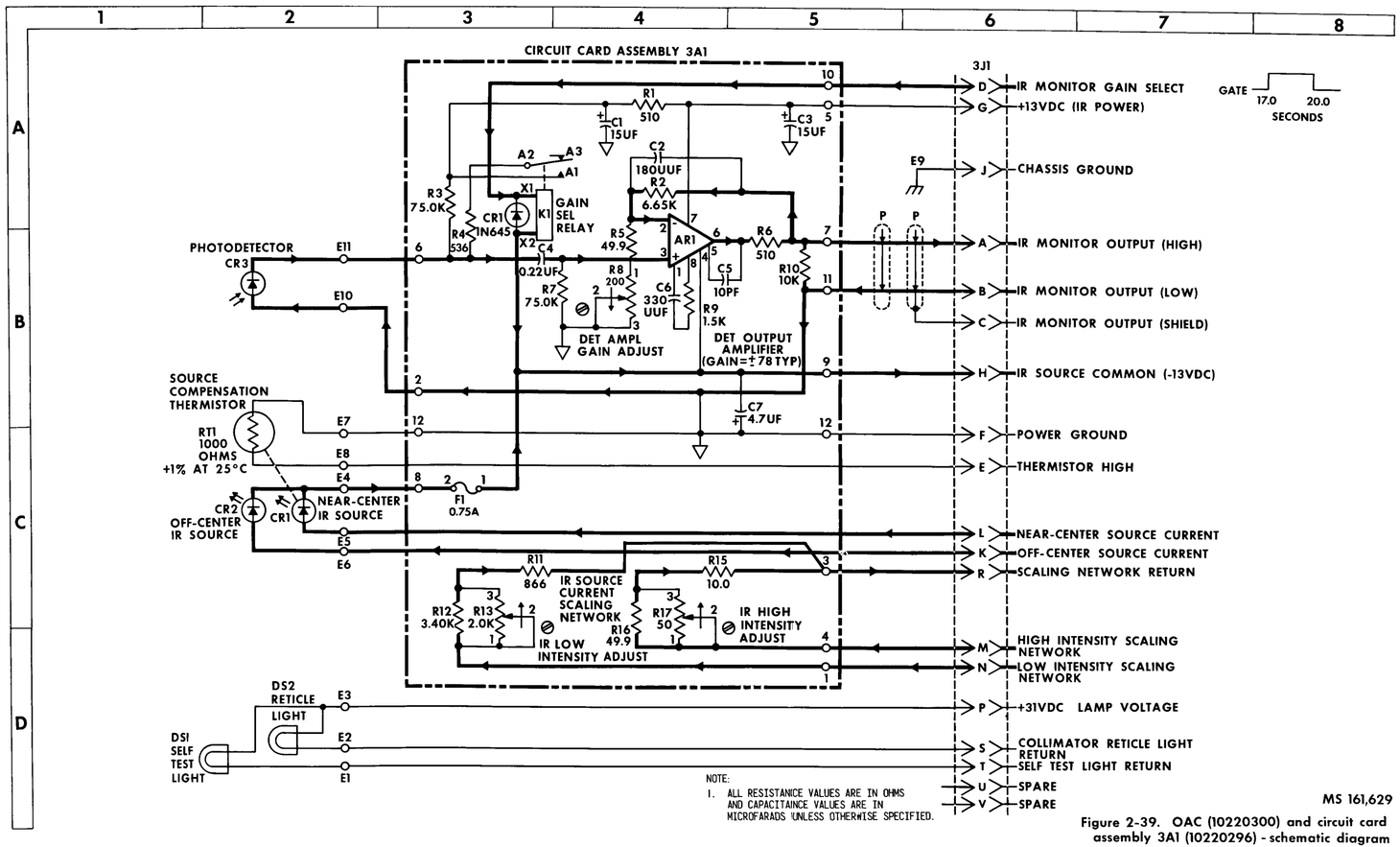
Figure 2-37. Optical alignment fixture - schematic diagram



1  3.0V-7.0V P-P 5.0V P-P NOM	6 1.5VDC TYPICAL (-1.25 TO -1.75VDC) IR SOURCE ANODE VOLTAGE CHANGE	11 SOURCE SELECT GATE 
2  NOMINAL INPUT= 1.0V(RMS)	7 SOURCE CURRENT ANALOG VOLTAGE V = 100 X CURRENT (LOW INTENSITY) V = 10 X CURRENT (HIGH INTENSITY)	
3 +13.0VDC (+12.7 TO +13.3VDC IN BS,) MC, ST AND TRAINER MODE	8 +3.8VDC (+3.6 TO 4.0VDC)	
4 IR INTENSITY SELECT GATE 	9 IR PULSE TRIGGER	12 +31VDC LAMP VOLTAGE (+28 TO +33VDC)
	10  IR PULSE CURRENT ANALOG 2.5V(TYP) 1.1 TO 6.0V -11.5 VDC	13 POWER GROUND
5 +13.0VDC (-12.7 TO -13.3VDC IN BS,) MC, ST AND TRAINER MODE		

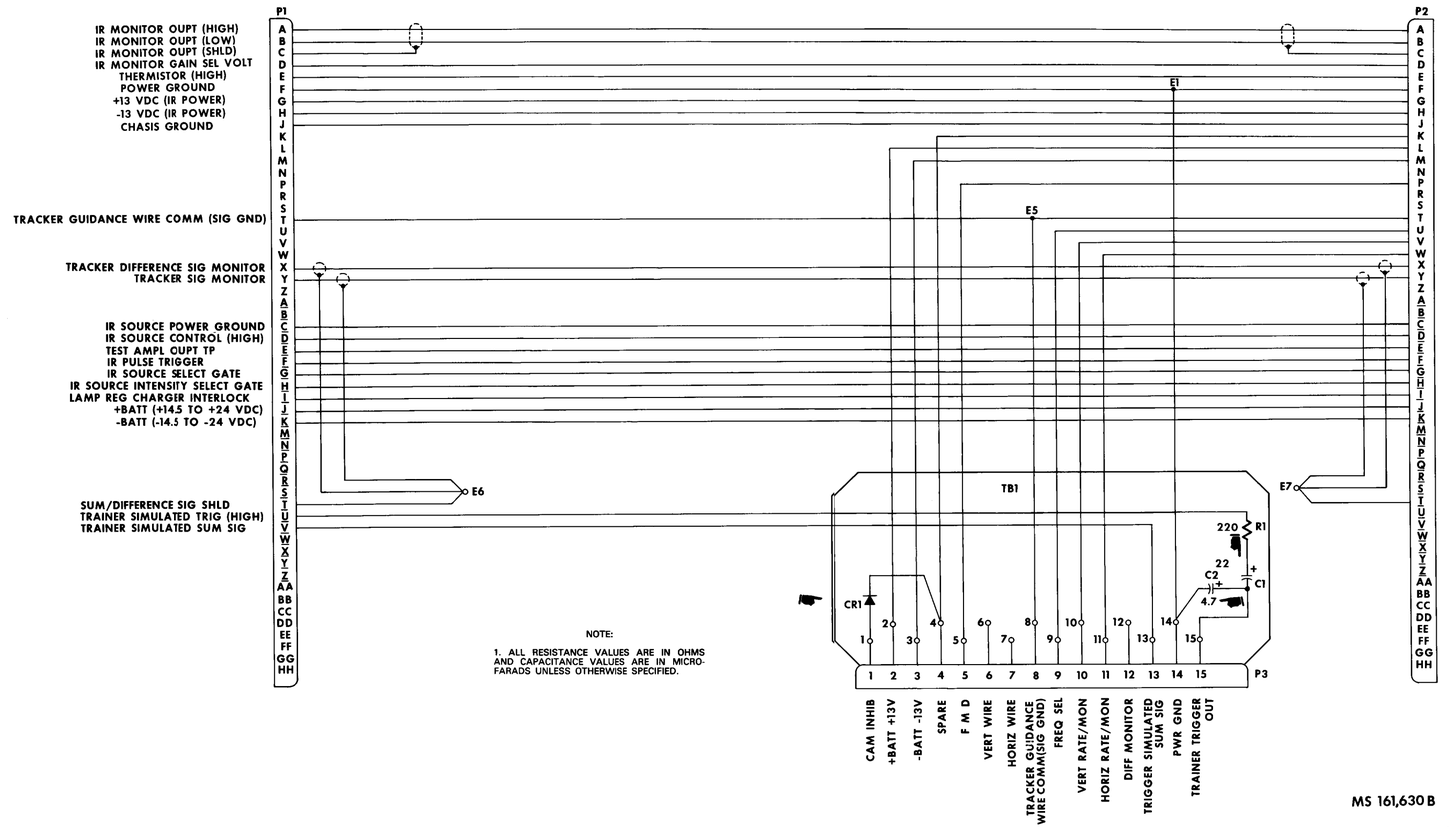
MS 161,628 A

Figure 2-38. Circuit card assembly 1A2A1 schematic diagram



MS 161,629

Figure 2-39. OAC (10220300) and circuit card assembly 3A1 (10220296) - schematic diagram



MS 161,630B

Figure 2-40. Circuit card assembly 1A4A1 schematic diagram

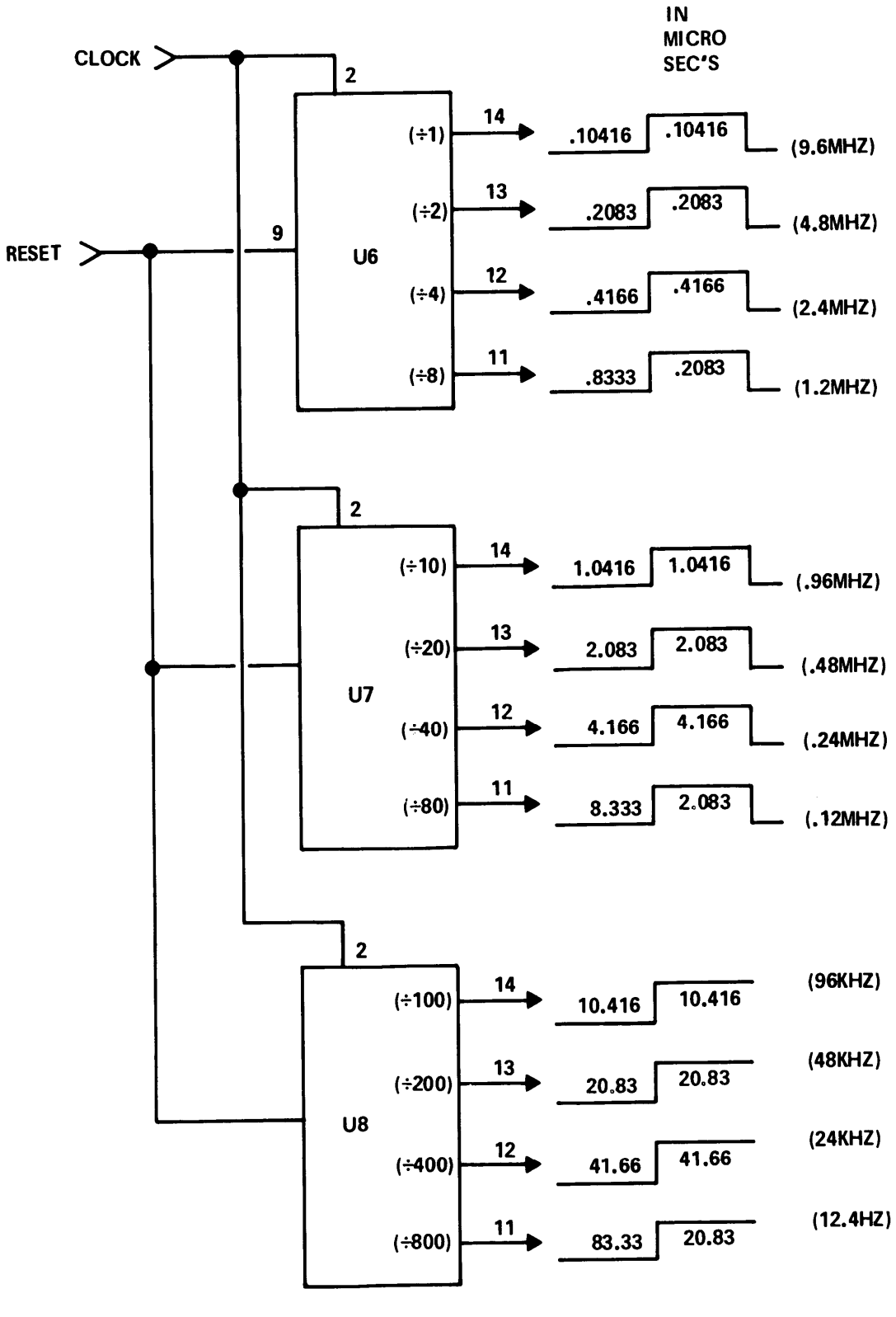
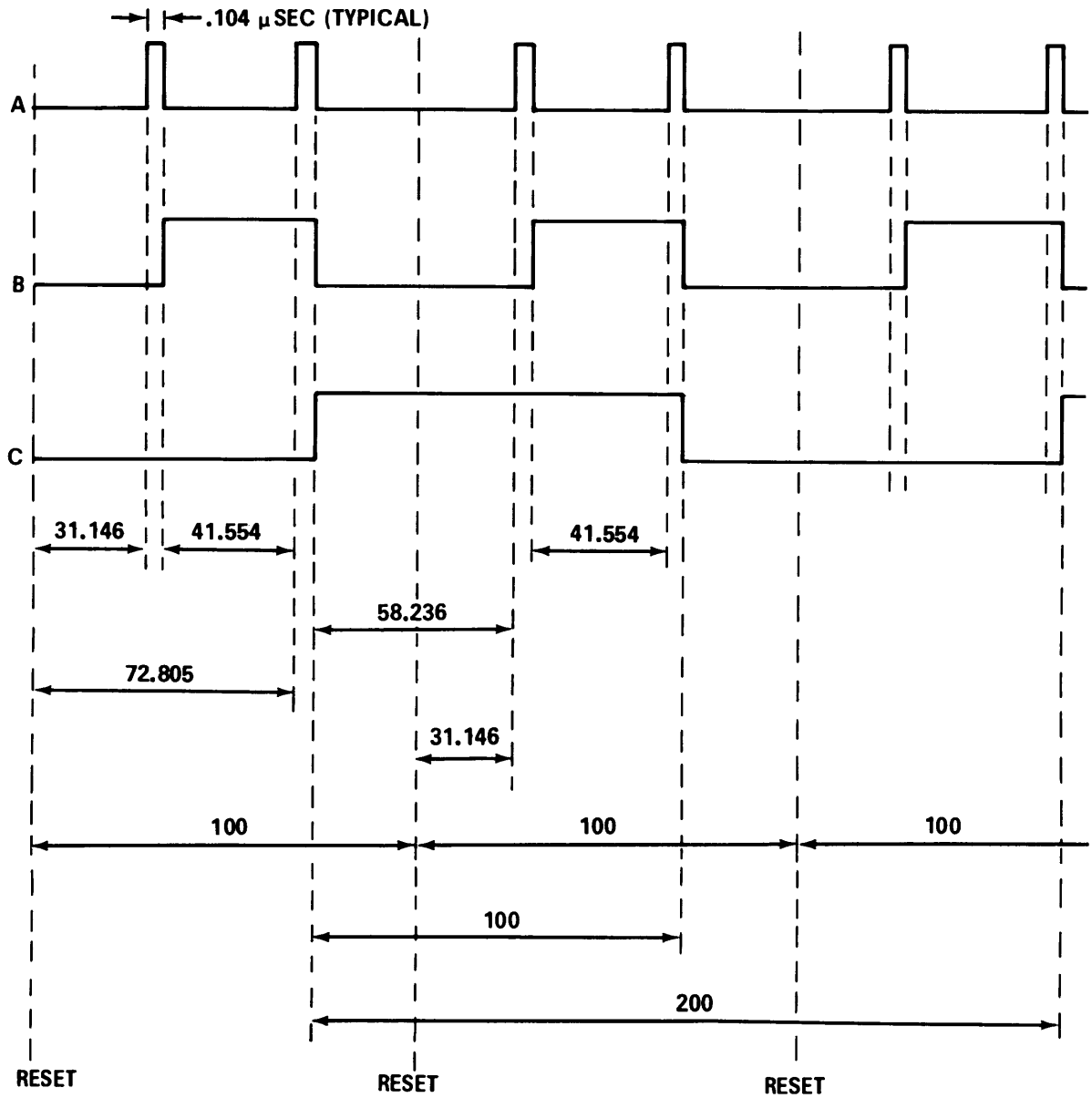


Figure 2–41 Circuit card assembly 1A8 decade counter outputs (U6,U7,U8)



NOTE: ALL ABOVE TIMES IN µ SECONDS.

MS 161,632

Figure 2–42 Circuit card assembly 1A8 comparator outputs (U2,U3, and U4)

CHAPTER 3
TROUBLESHOOTING

3-1. Special Tools and Equipment.

Special tools and equipment used in servicing and testing the TTS are listed in TM 9-4935-481-14-1.

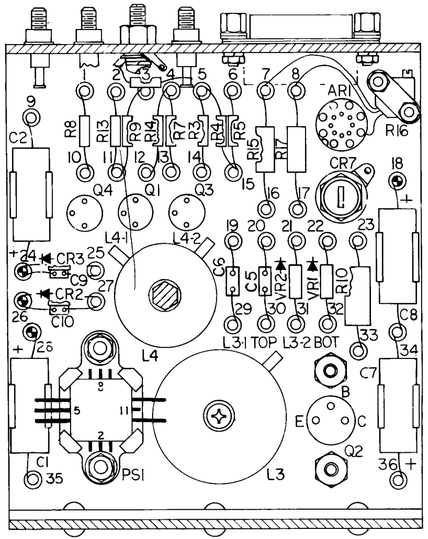
3-2. Troubleshooting Procedures.

a. Operating and self-test procedures for the TTS are contained in TM 9-4935-480-14.

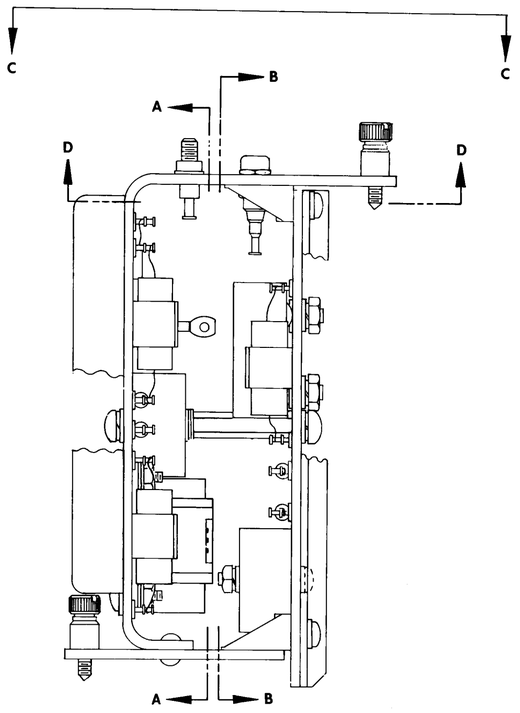
b. Procedures for testing, adjusting, calibrating, and troubleshooting the TTS are contained in TM 9-4935-481-14-1.

c. Refer to the diagrams in Chapter 2, and to the component location diagrams in this chapter to supplement the check procedures in TM 9-4935-481-14-1.

d. Refer to chapter 4 for subassembly removal, repair, and replacement procedures.

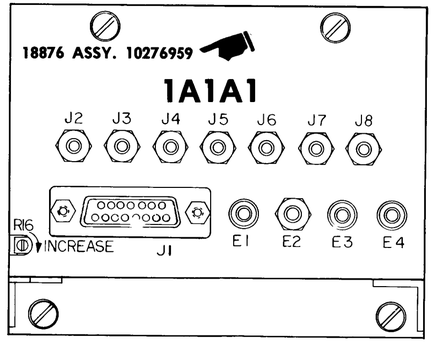


SECTION A-A

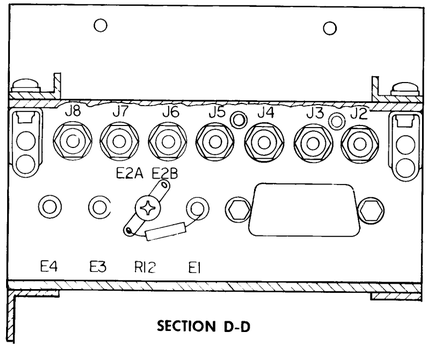


MS161,633A

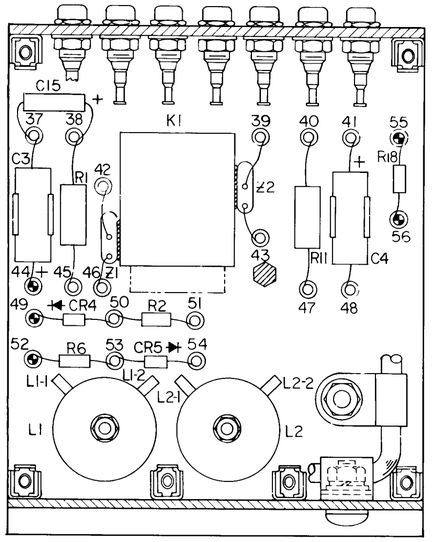
Figure 3-1. Circuit card assembly 1A1A1 - locational diagram (sheet 1 of 2)



SECTION C-C



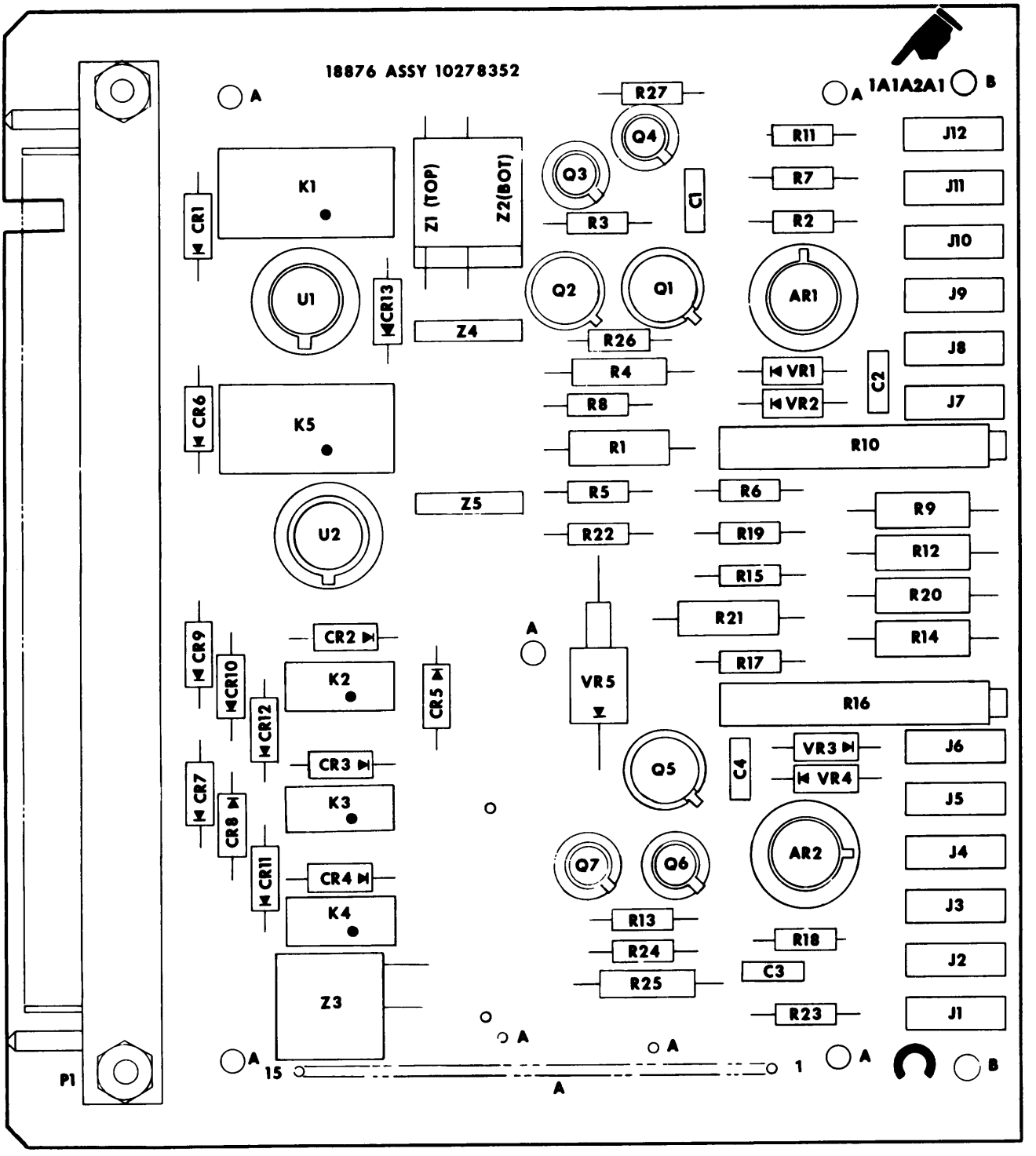
SECTION D-D



SECTION B-B

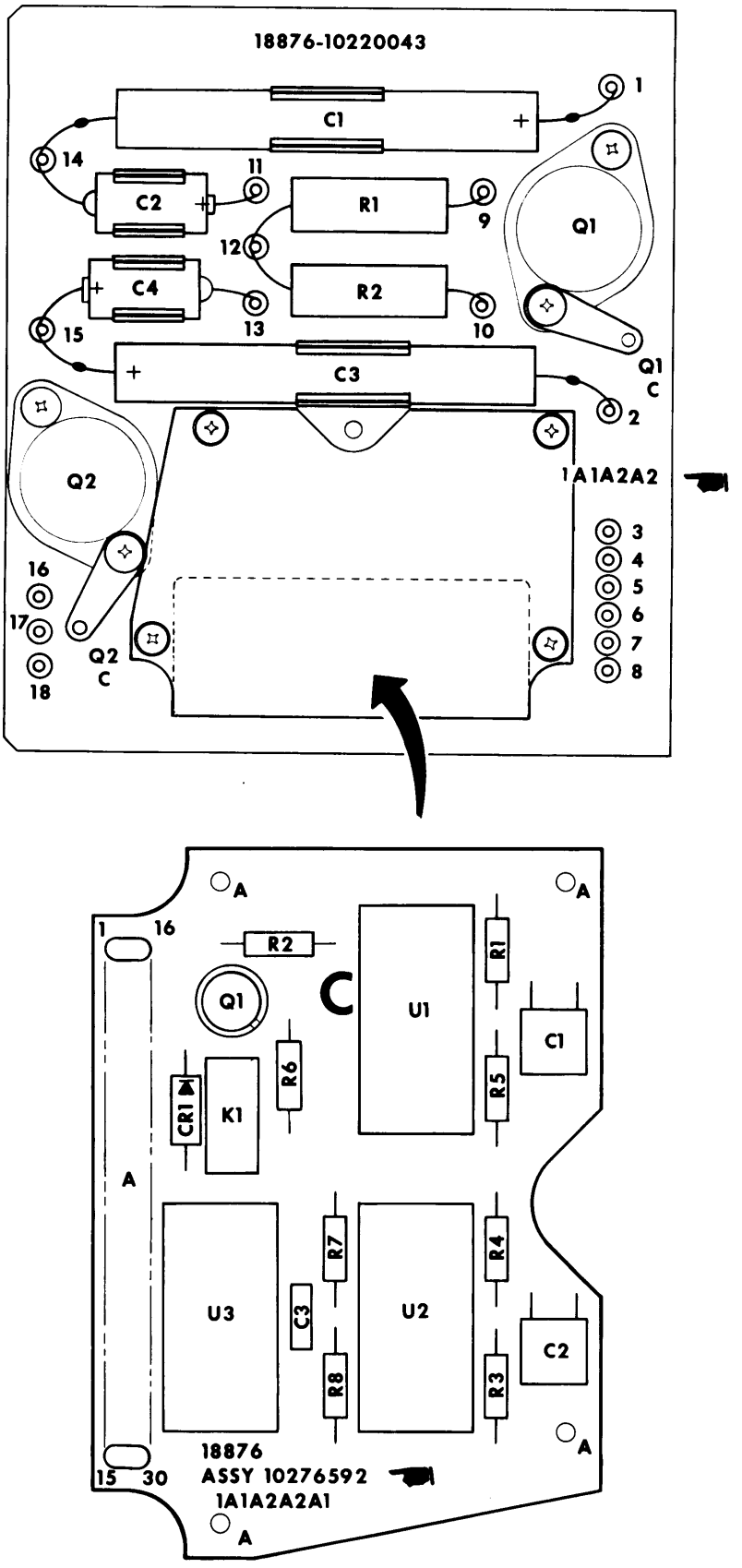
MS 161,634A

Figure 3-1. Circuit card assembly 1A1A1 - location diagram (sheet 2 of 2)



MS 161,635 A

Figure 3-2. Circuit card assembly 1A1A2A1 - locational diagram



MS 161,636 A

Figure 3-3. Circuit card assembly 1A1A2A2 - locational diagram

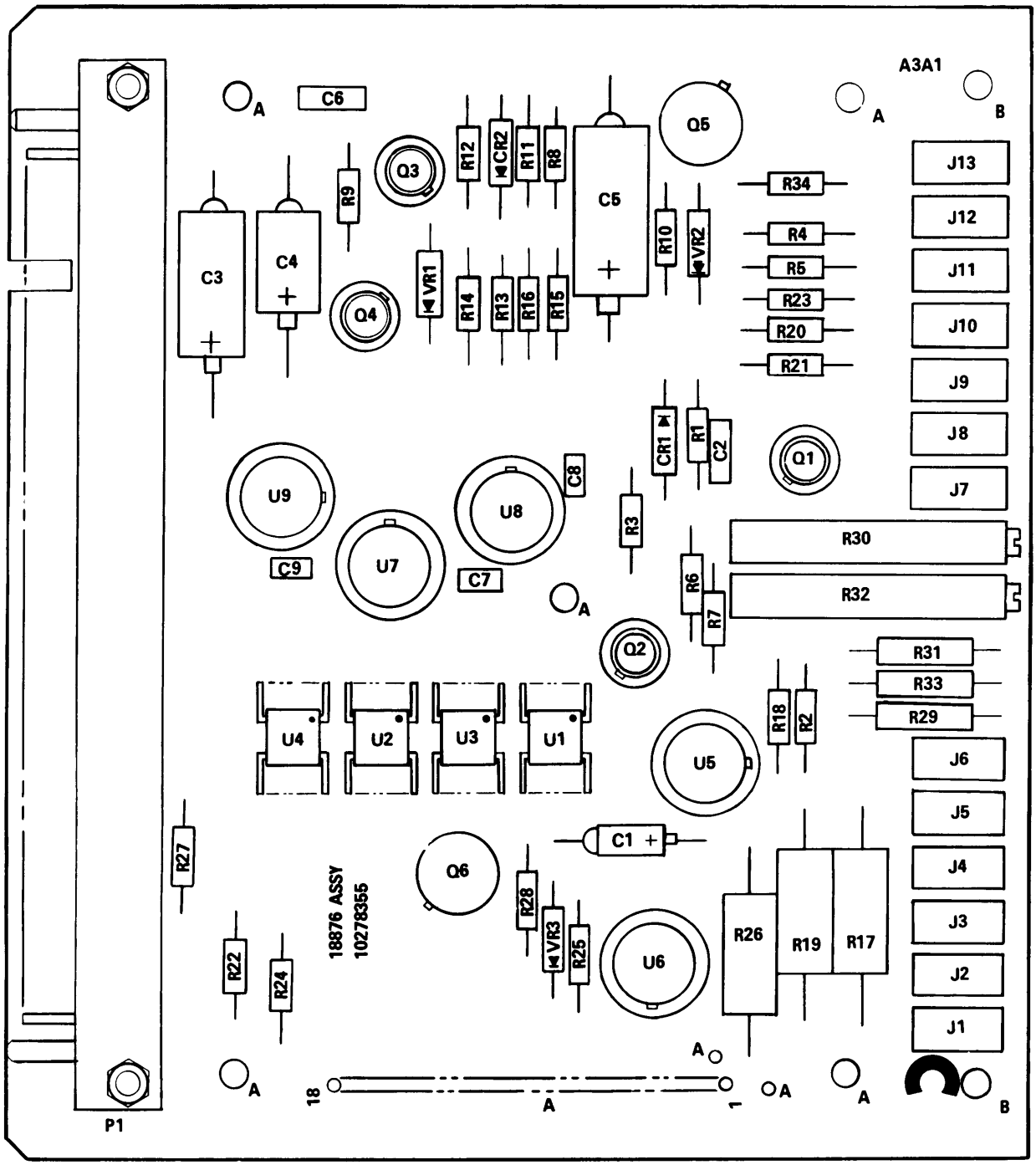


Figure 3-4. Circuit card assembly 1A3A1 (10278355) - locational diagram

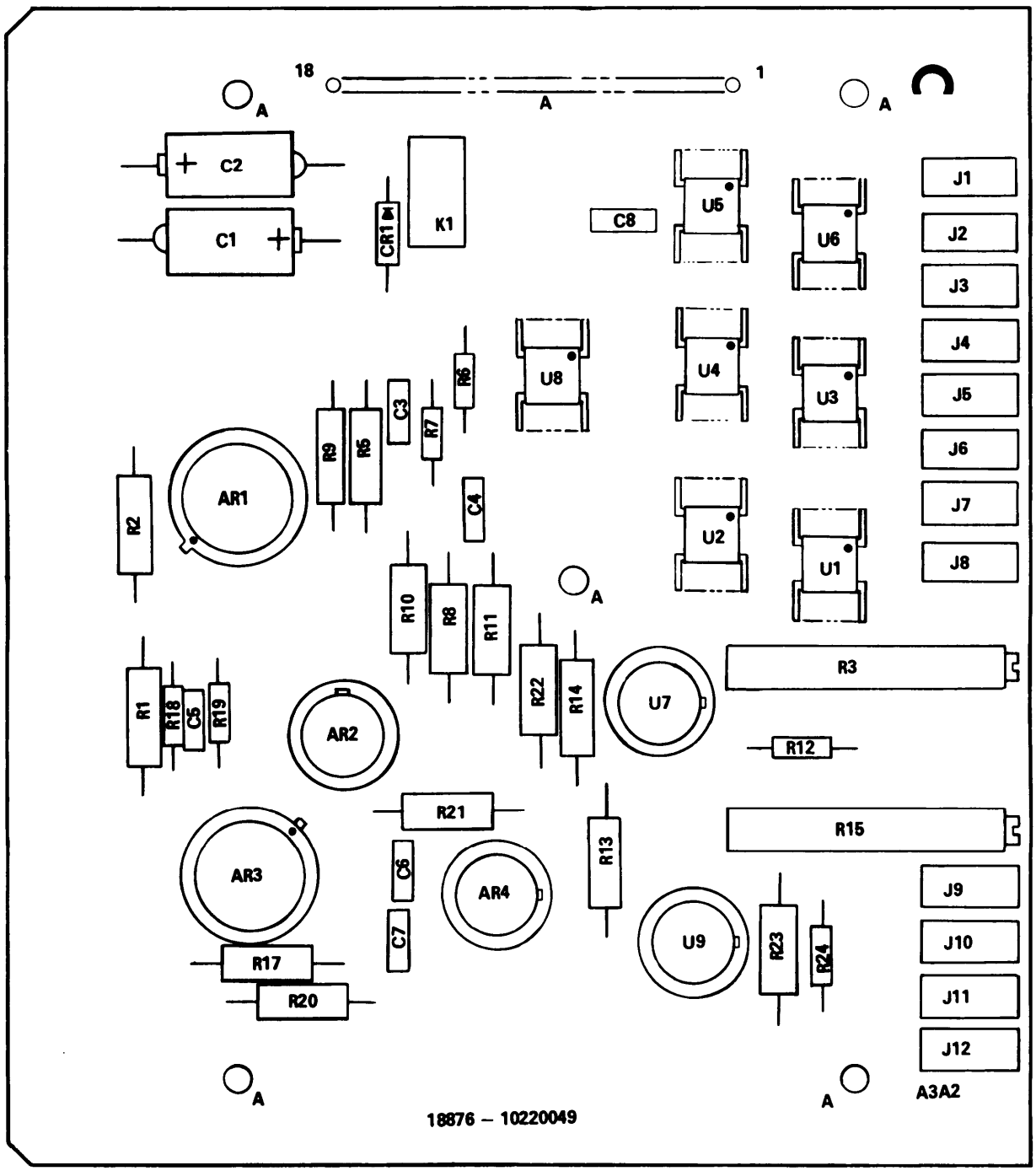


Figure 3-5. Circuit card assembly 1A3A2 (10220049) - locational diagram

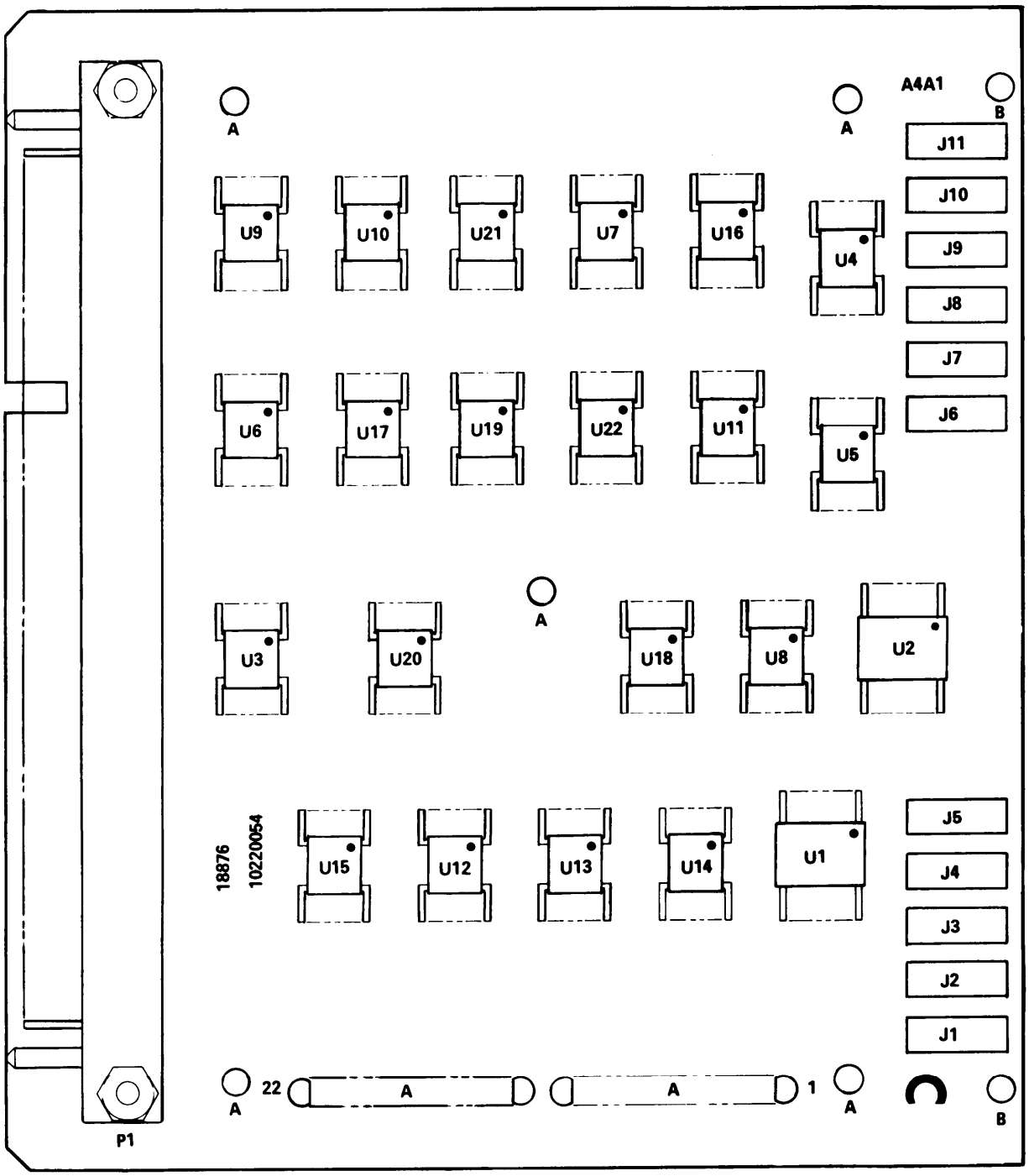


Figure 3-6. Circuit cord assembly 1A4A1 (10220054) - locational diagram

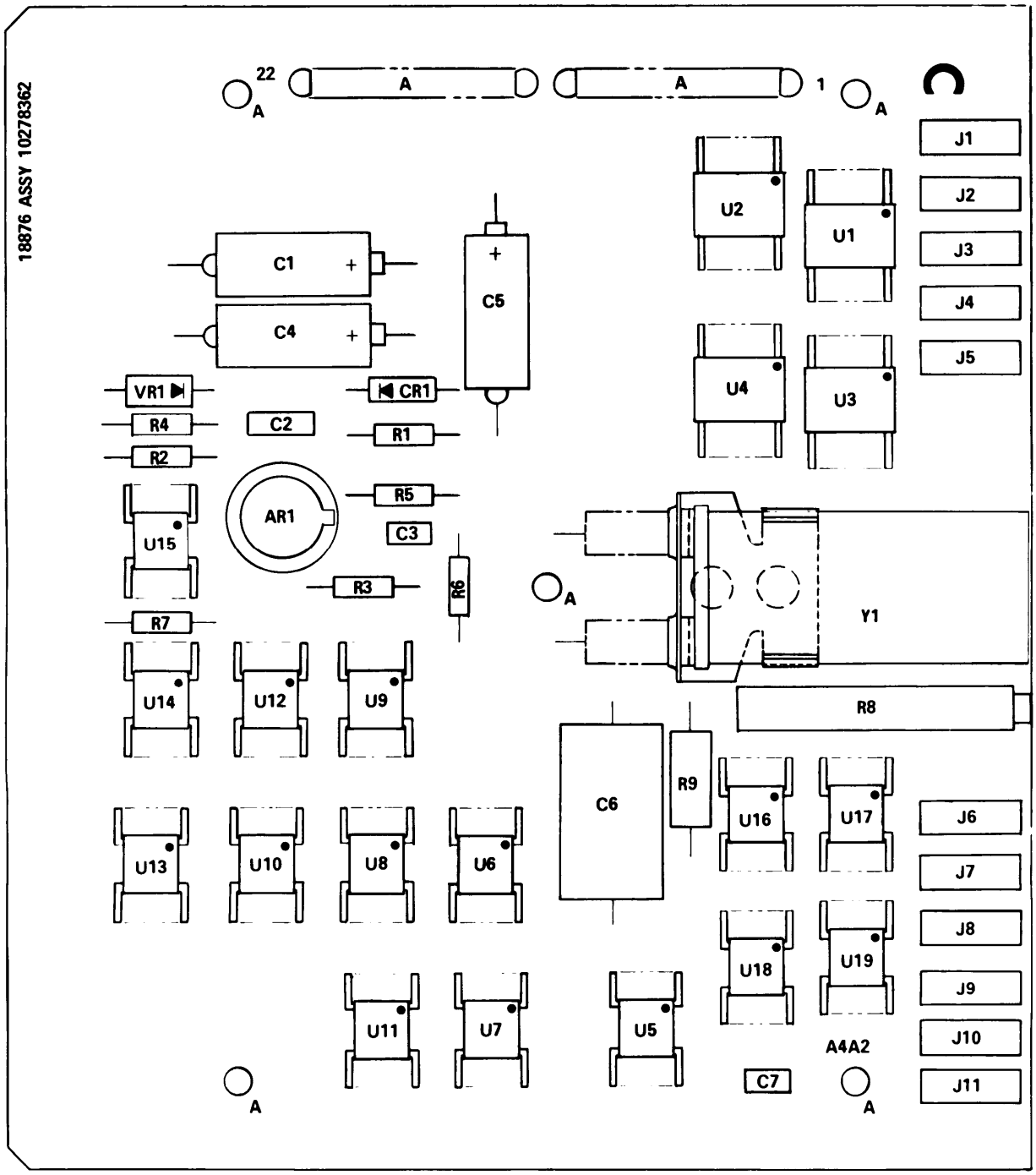


Figure 3-7. Circuit card assembly 1A4A2 (10278362) - locational diagram

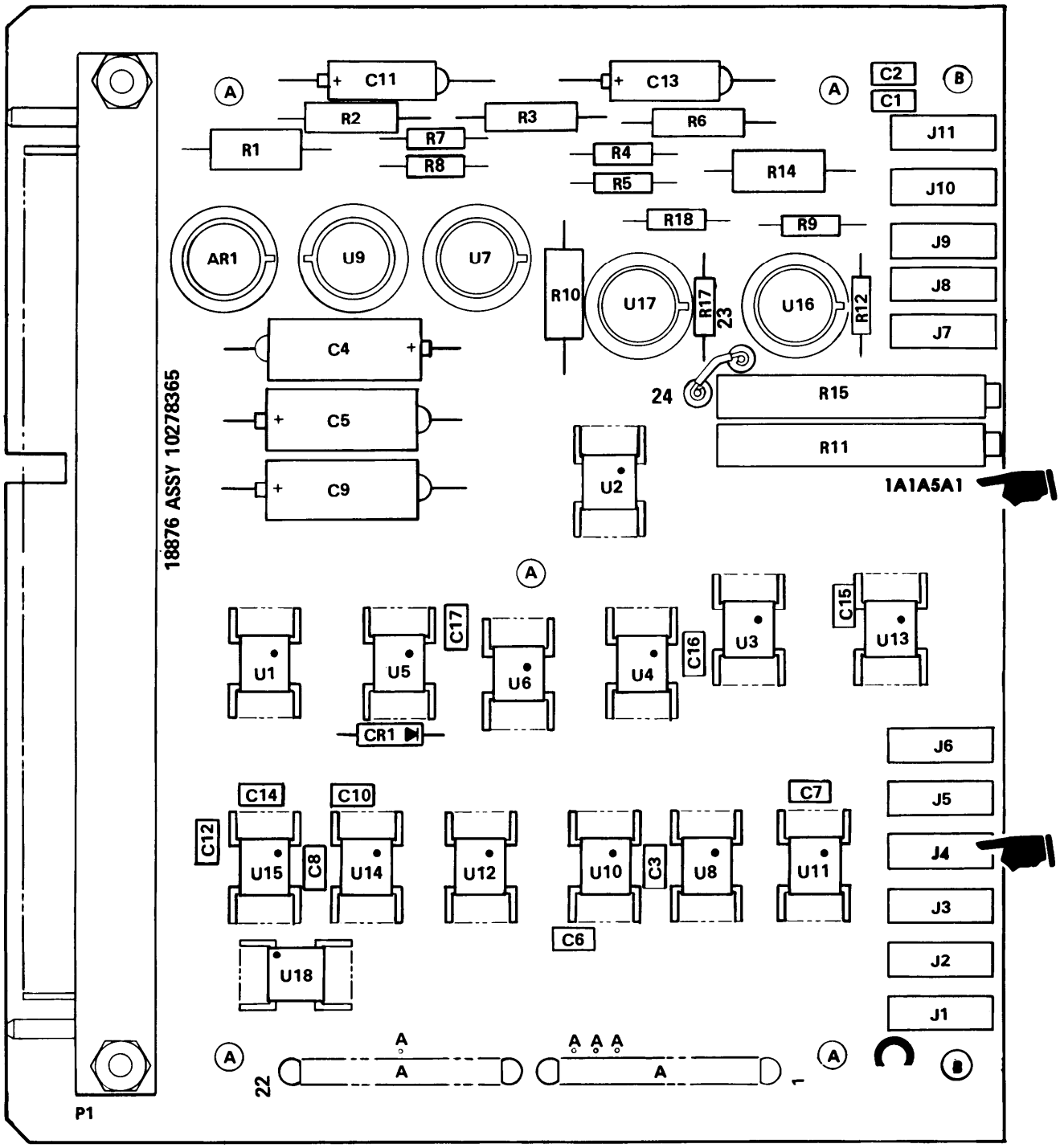


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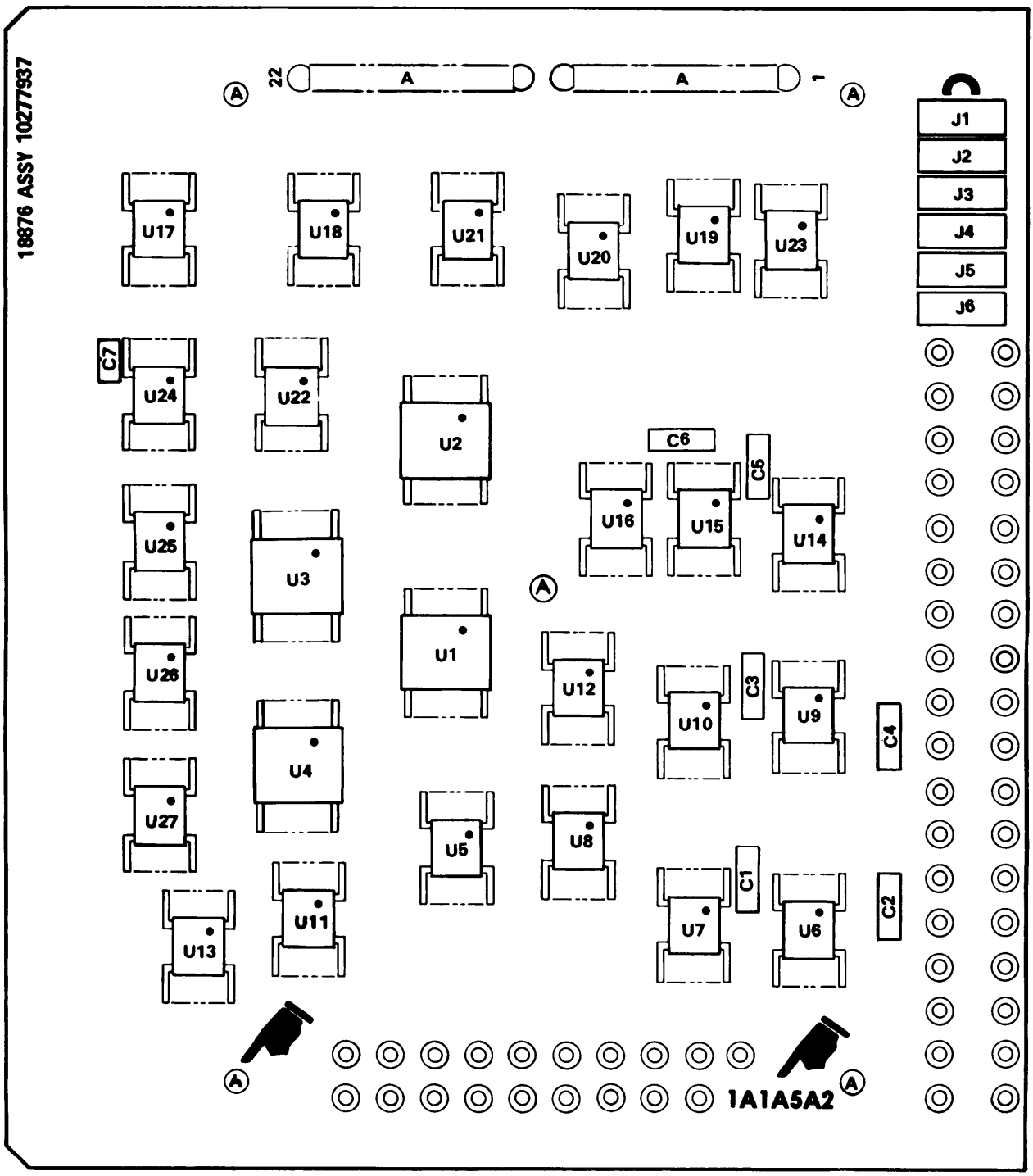
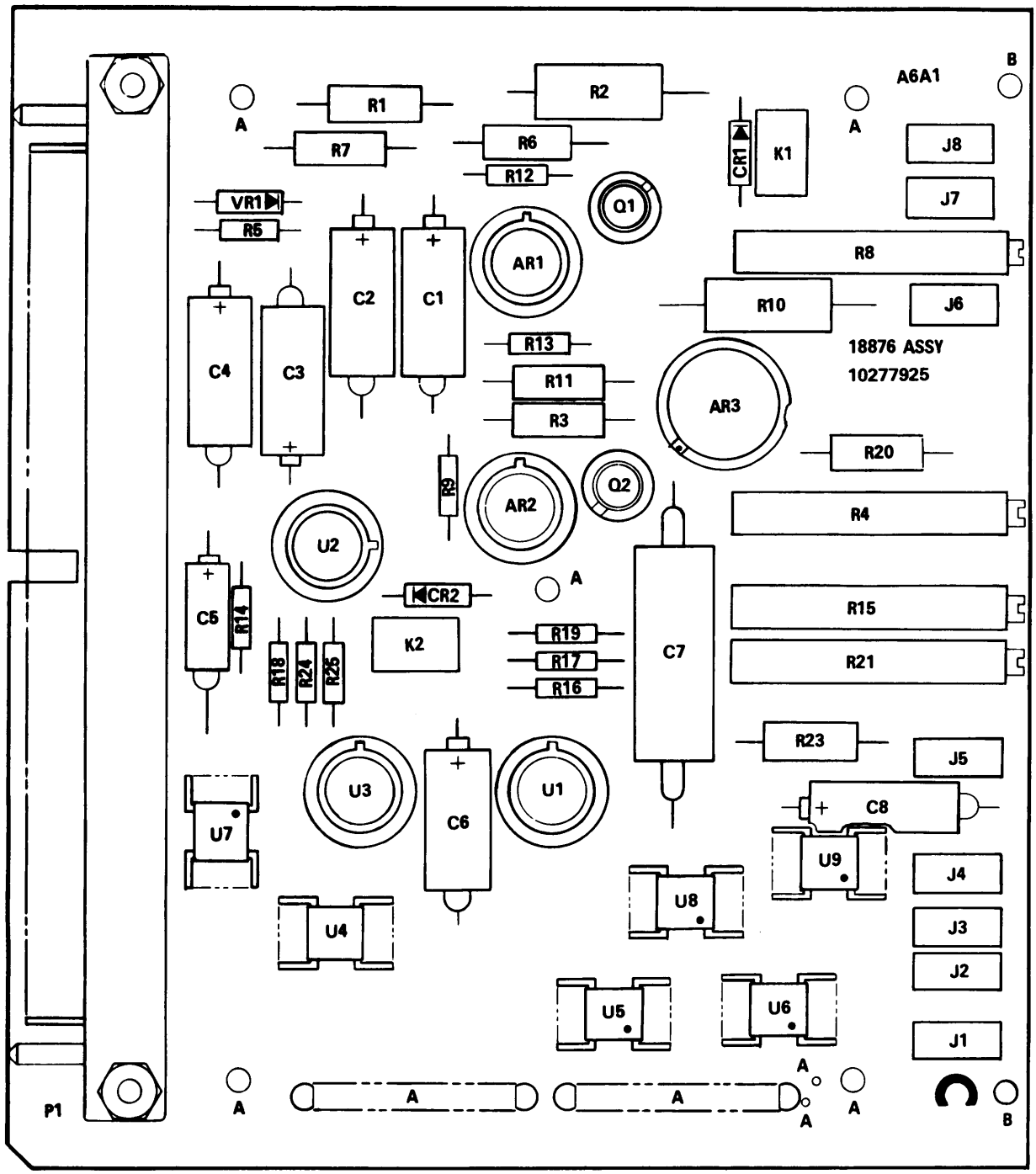
Figure 3-8. Circuit card assembly 1A1A5A1 - locational diagram



MS 161,642 A

Figure 3-9. Circuit card assembly 1A1A5A2 - locational diagram



MS 161,643

Figure 3-10. Circuit card assembly 1A6A1 (10277925) - locational diagram

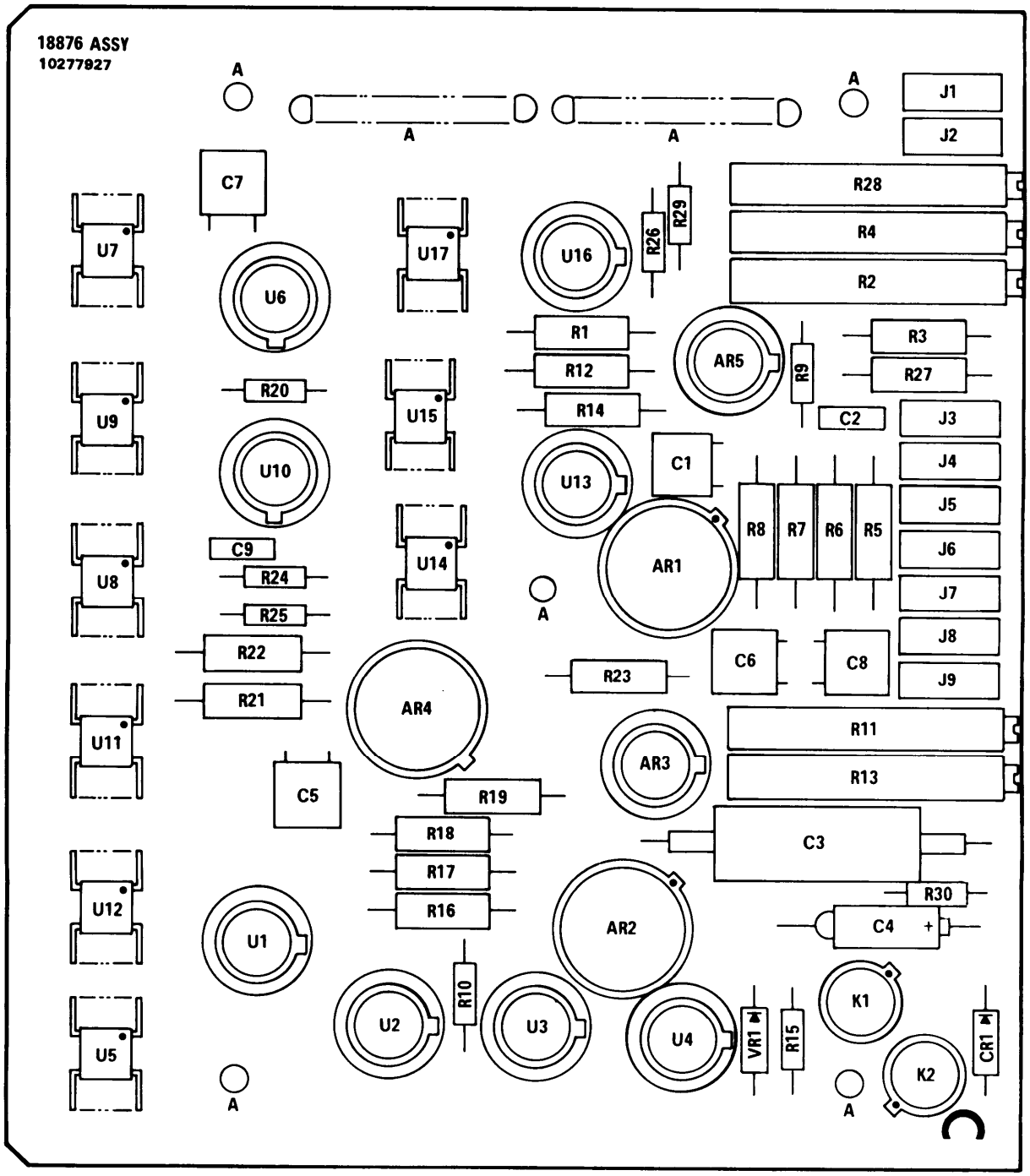


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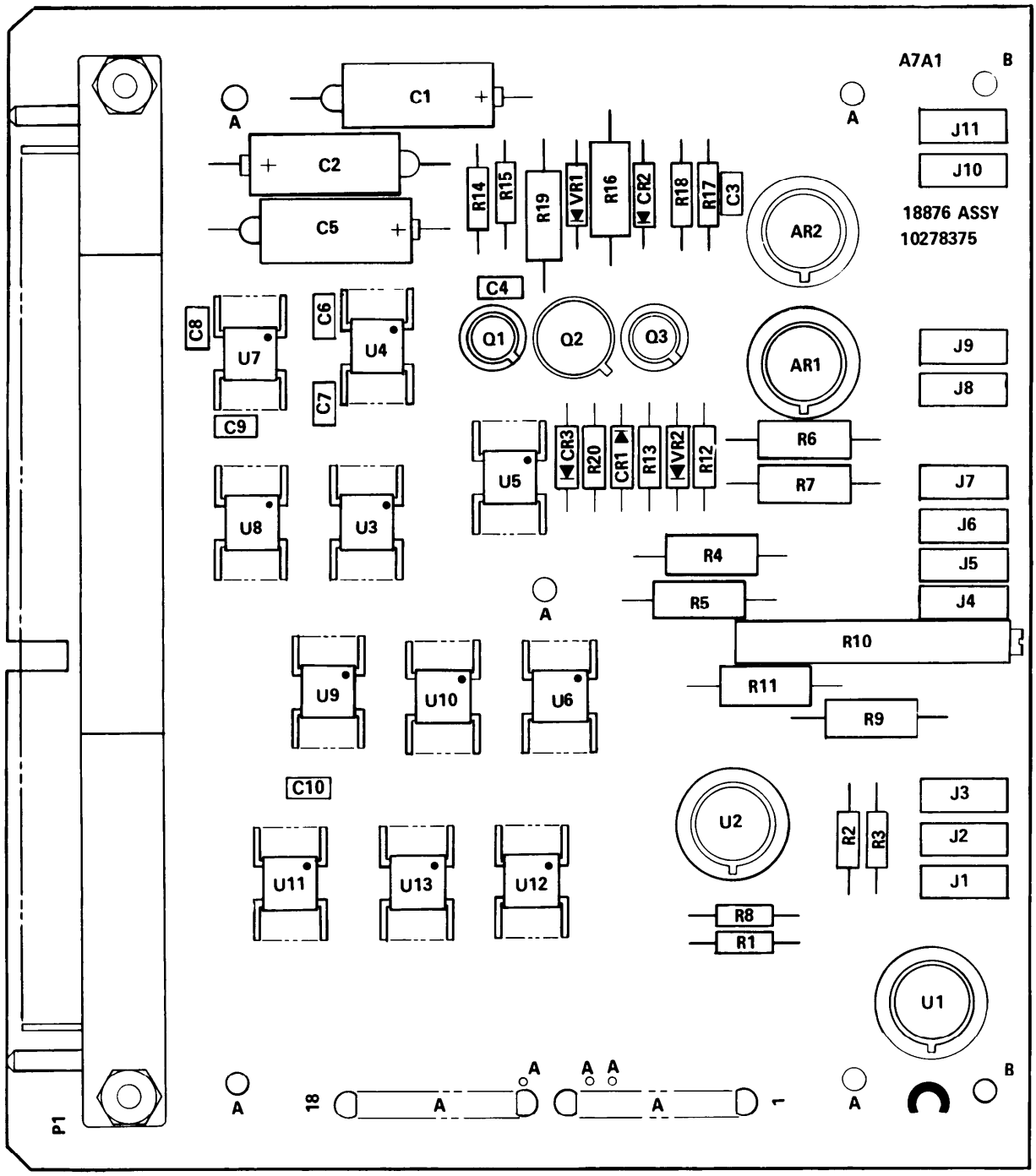
Figure 3-11. Circuit card assembly 1A6A2 (10277927) - locational diagram



MS 161,645

Figure 3-12. Circuit card assembly 1A7A1 (10278375) - locational diagram

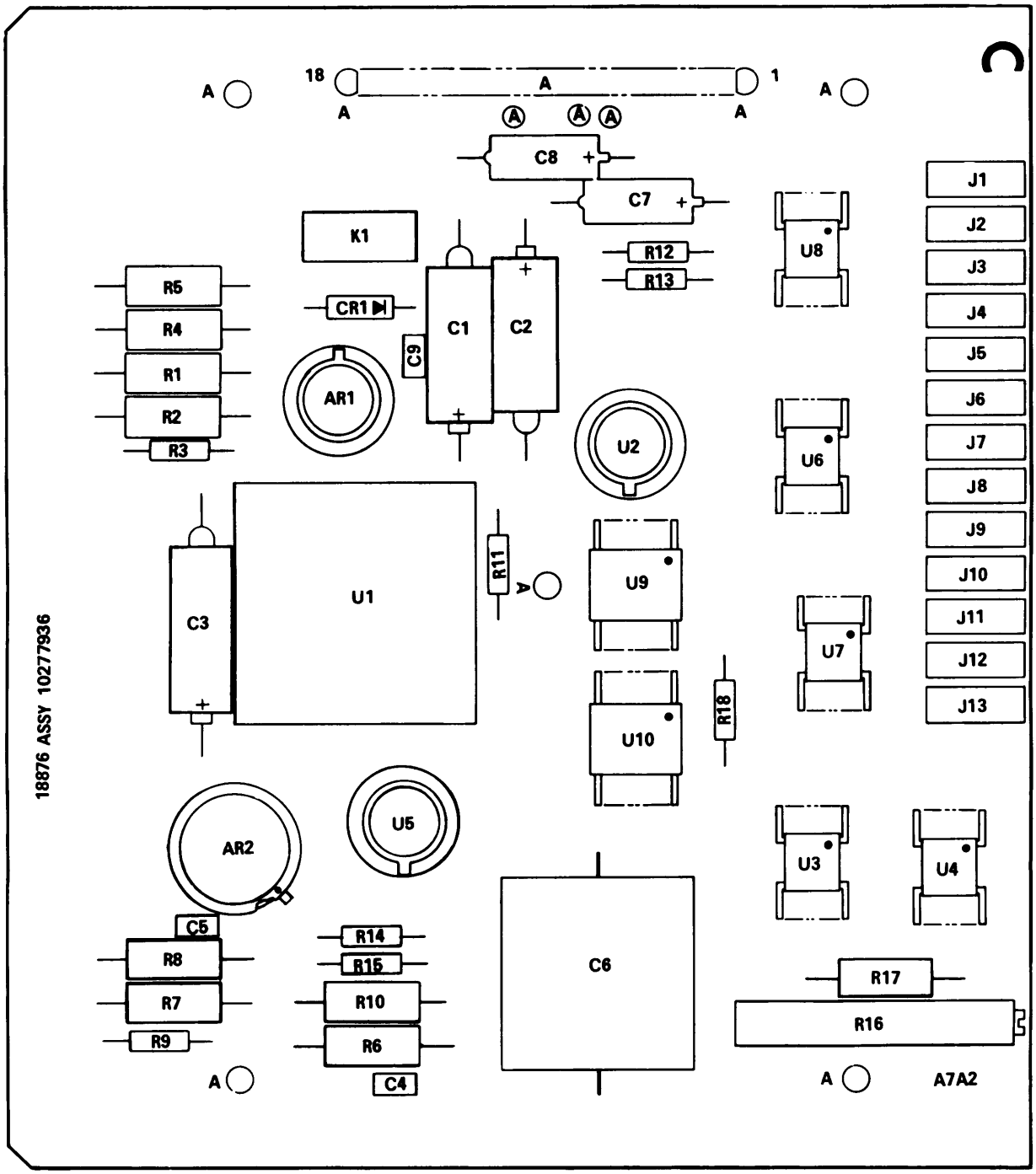
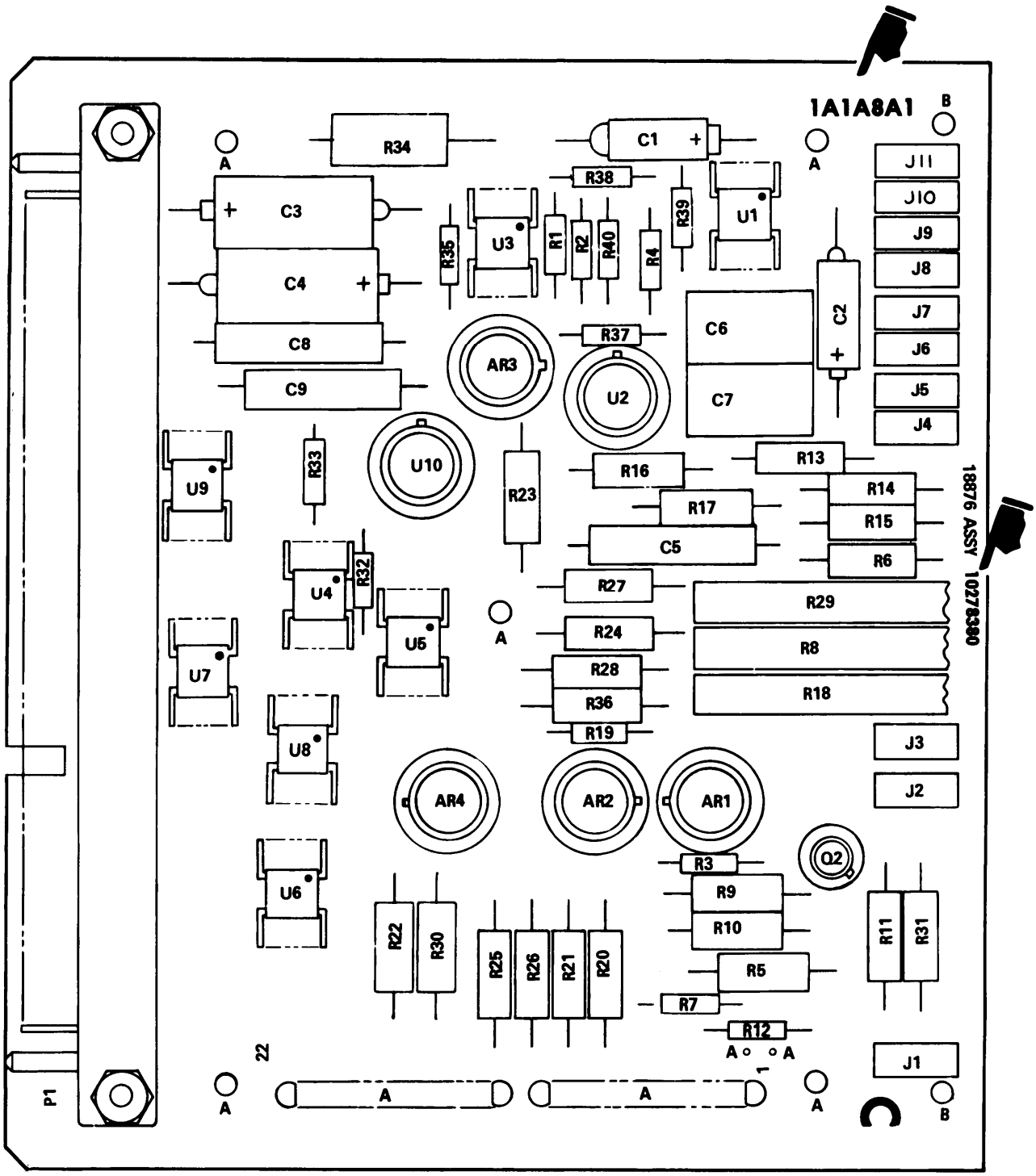


Figure 3-13. Circuit card assembly 1A7A2 (10277936) - locational diagram



MS 161,647 A

Figure 3-14. Circuit card assembly 1A1A8A1 - locational diagram

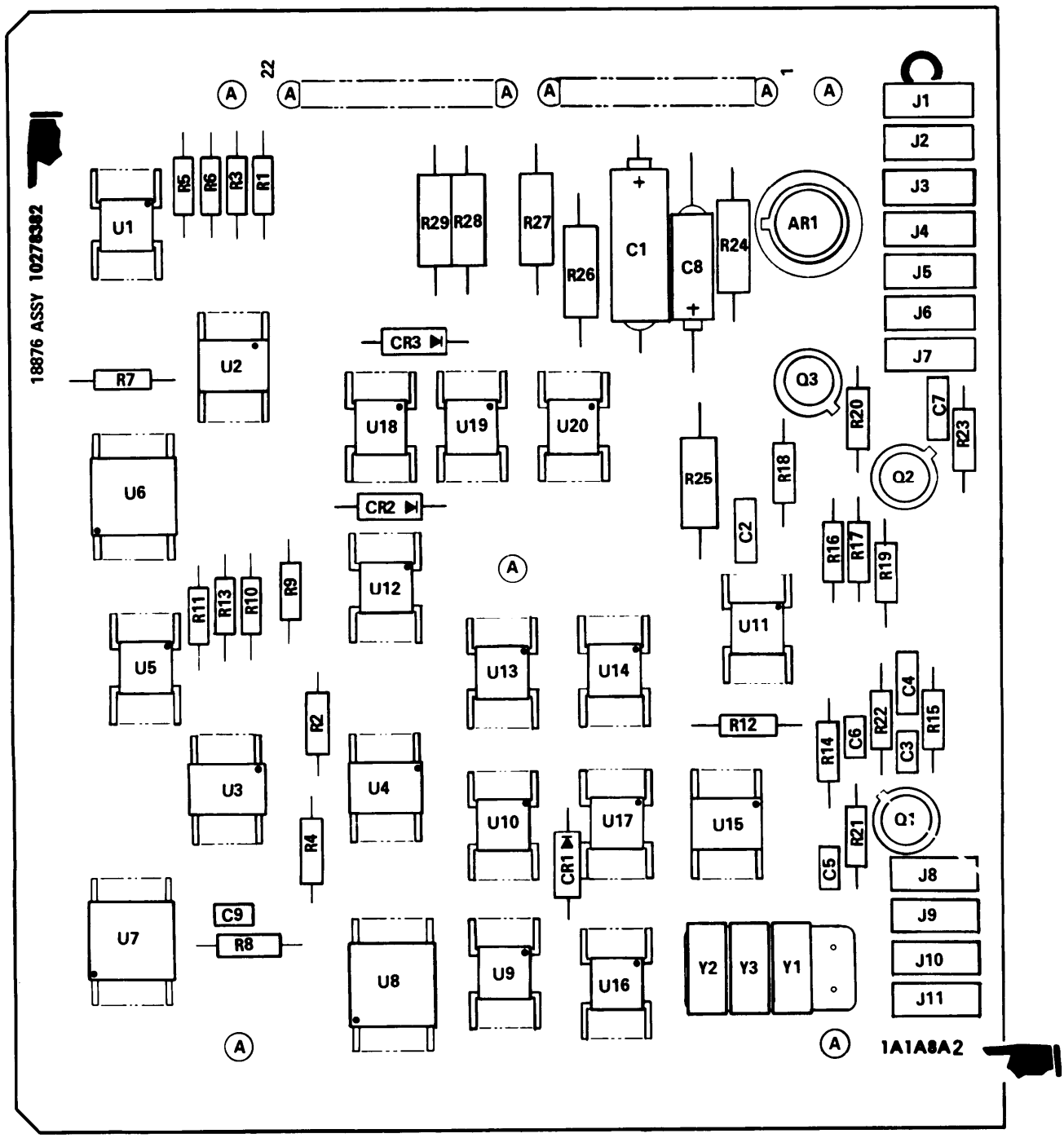


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Figure 3-15. Circuit card assembly 1A1A8A2 - locational diagram

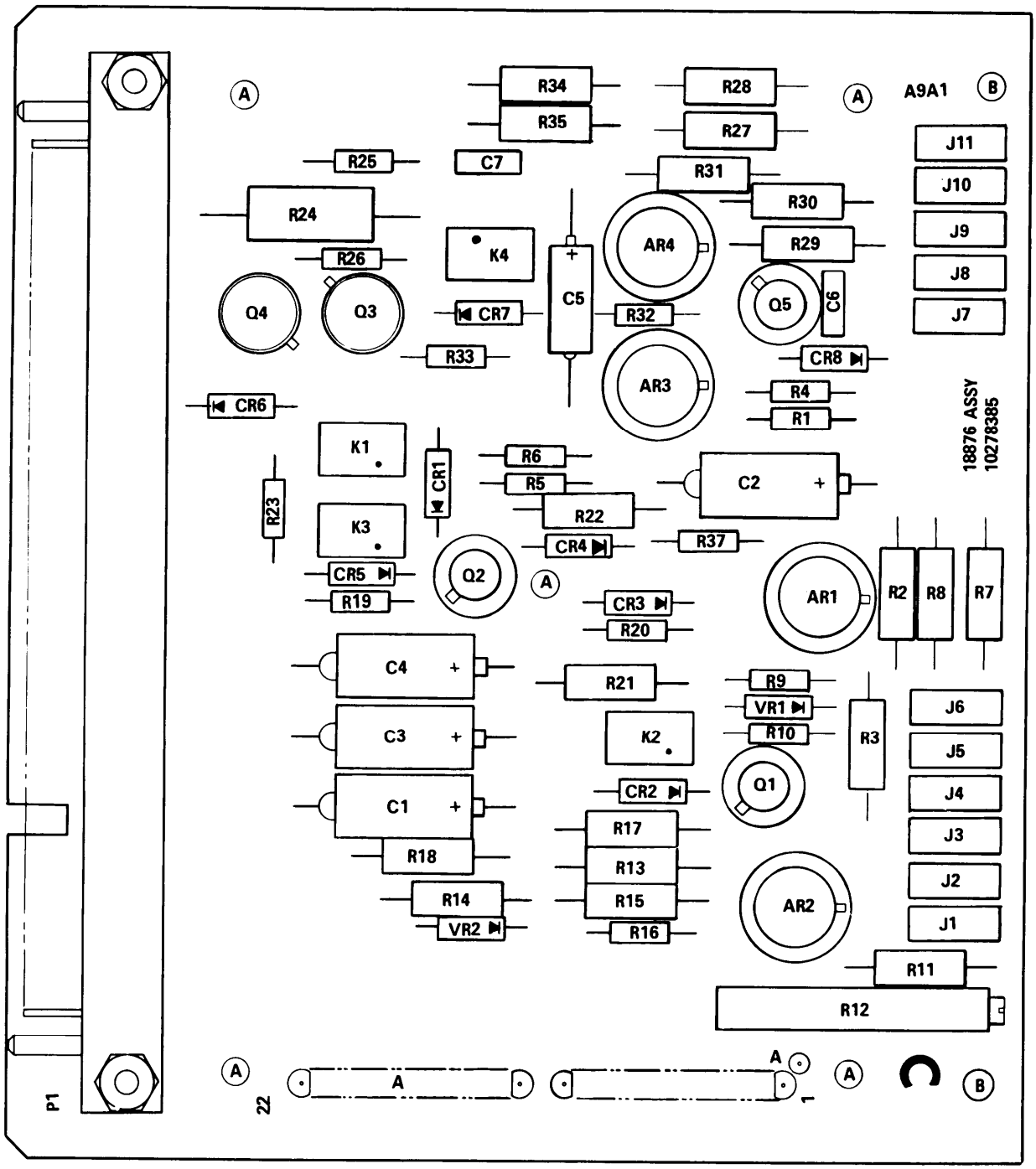


Figure 3-16. Circuit card assembly 1A9A1 (10278385) - locational diagram

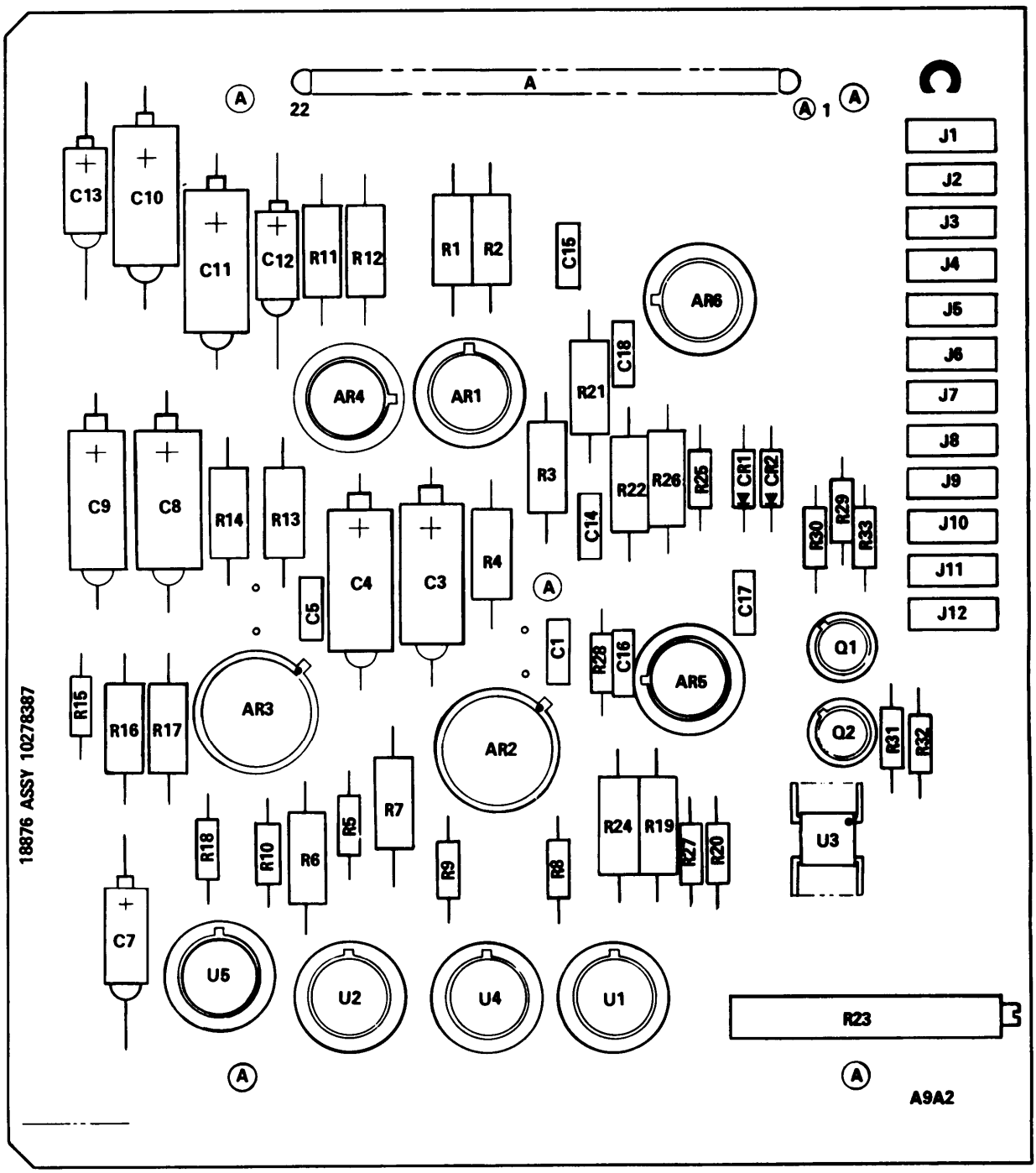
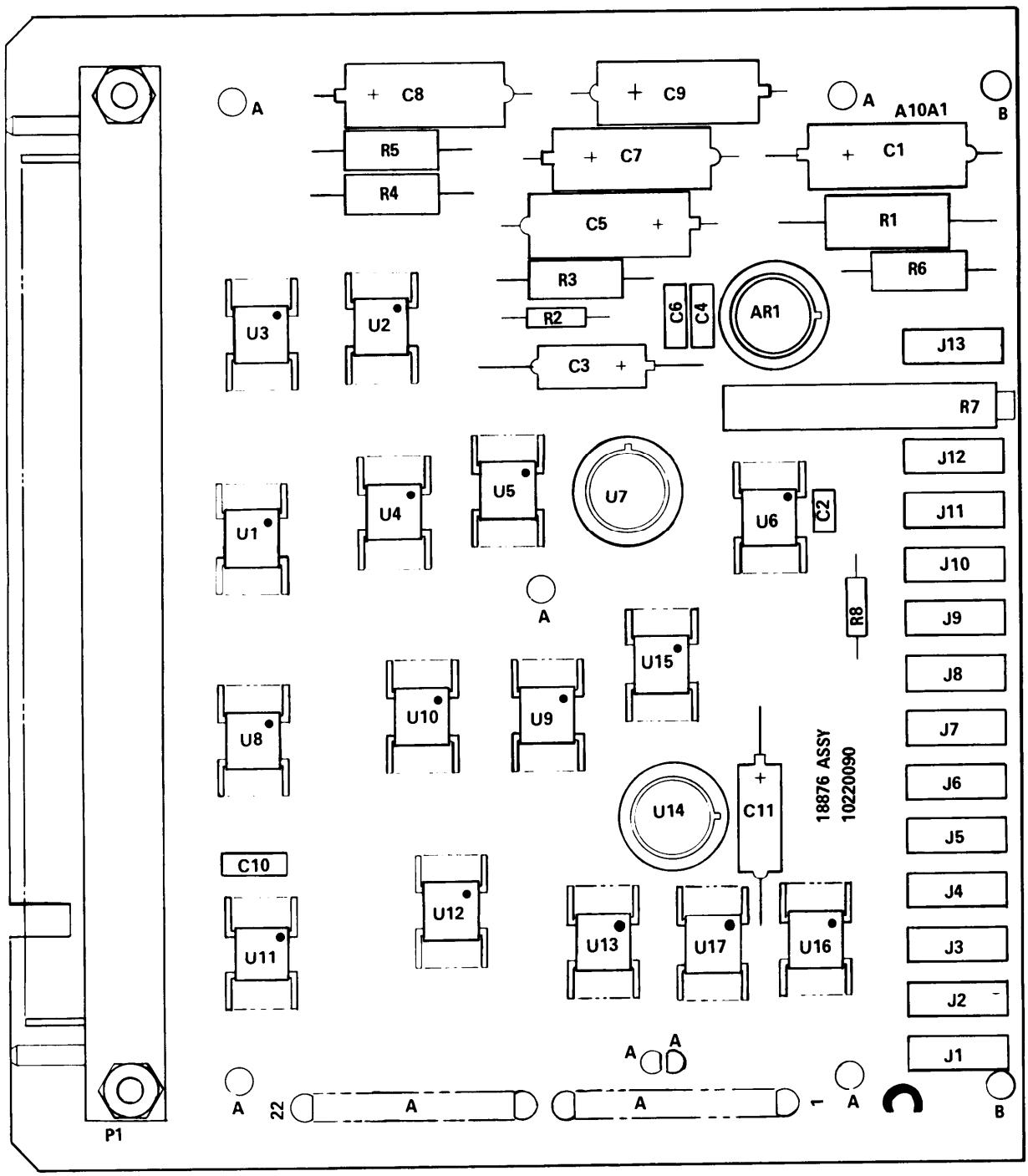
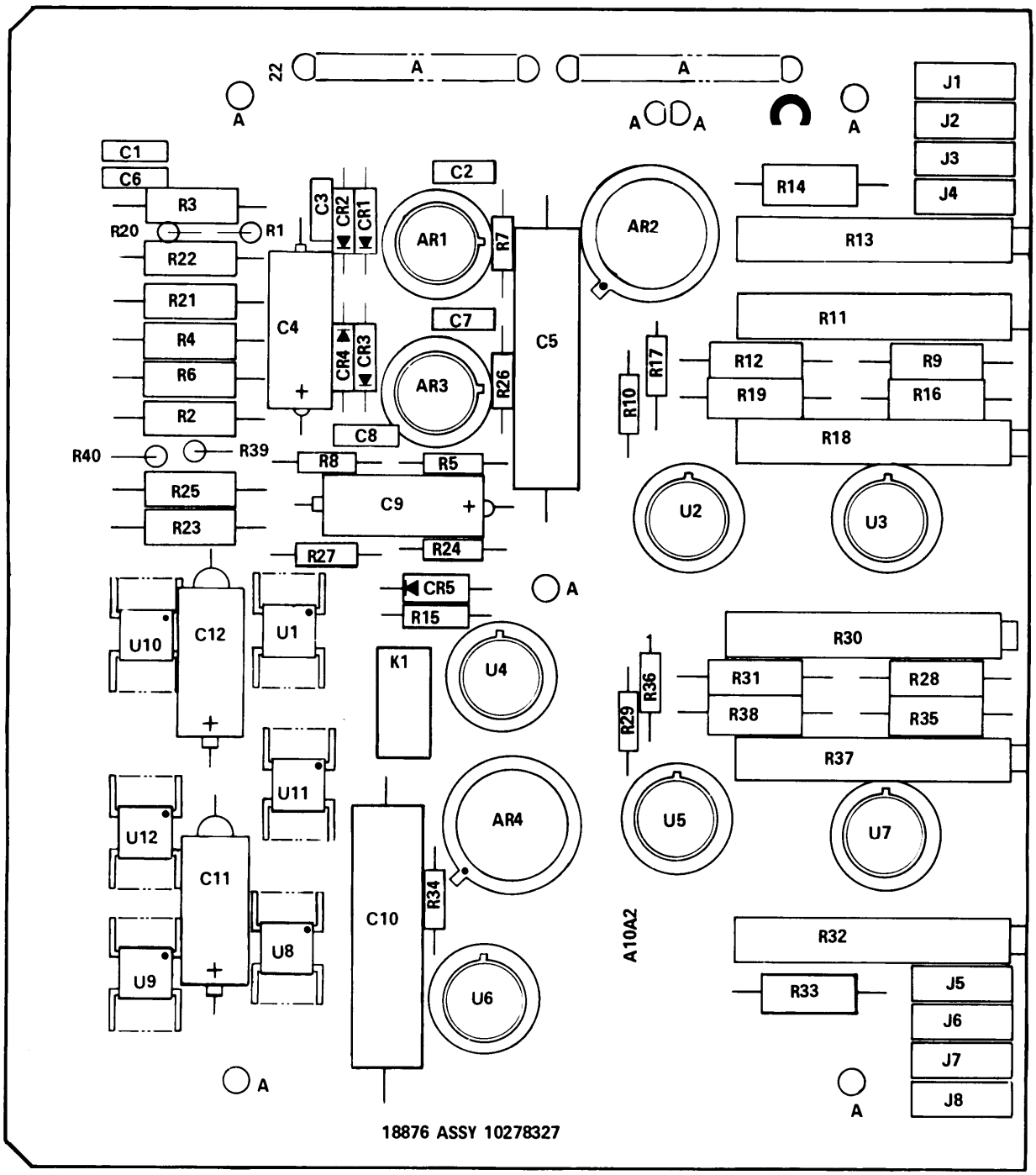


Figure 3-17. Circuit card assembly 1A9A2 (10278387) - locational diagram



MS 161,651

Figure 3-18. Circuit card assembly 1A10A1 (10220090) - locational diagram



MS 161,652

Figure 3-19 Circuit card assembly 1A10A2 (10278327) - locational diagram

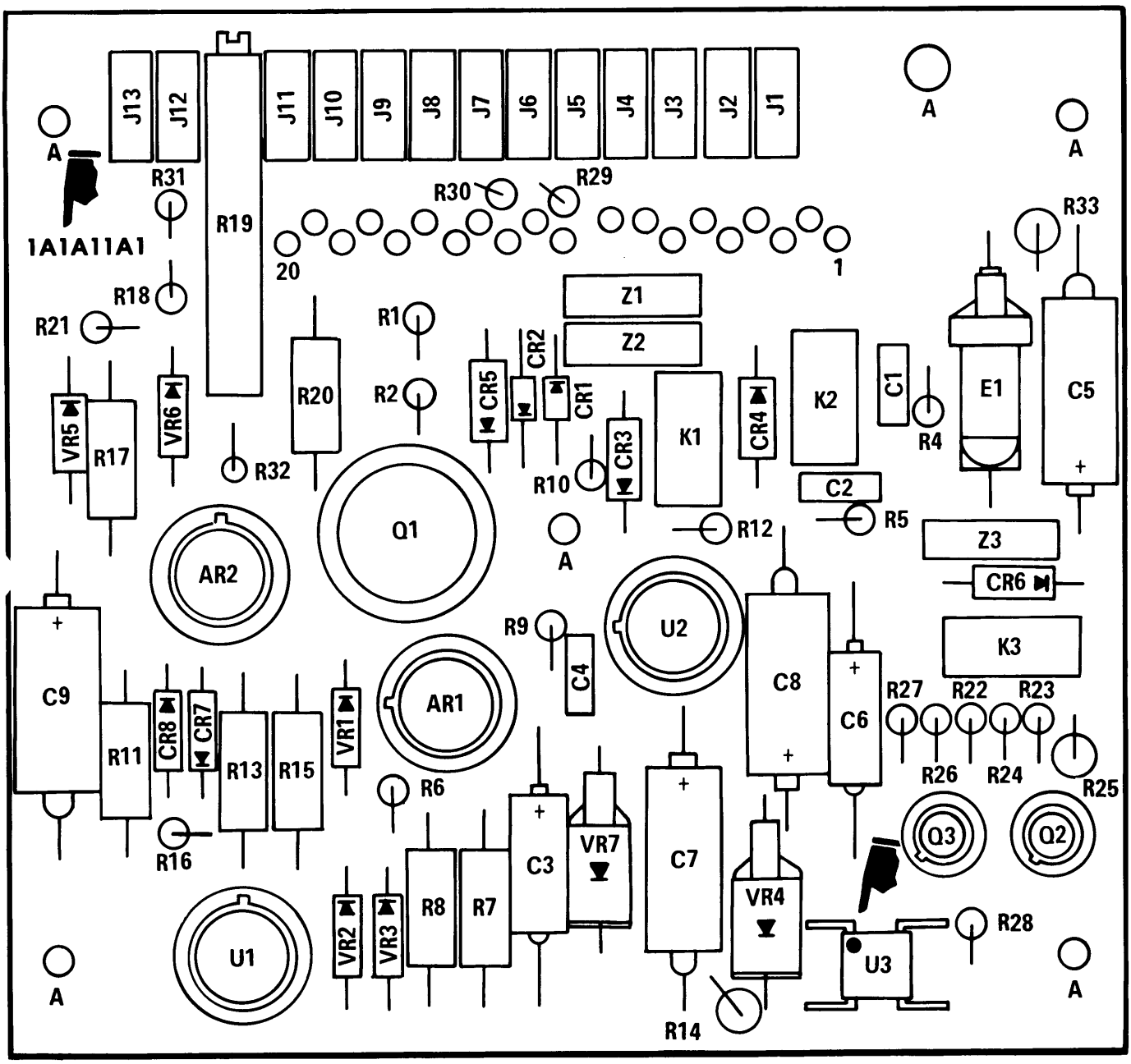


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Figure 3-20. Circuit card assembly 1A1A11A1 - locational diagram

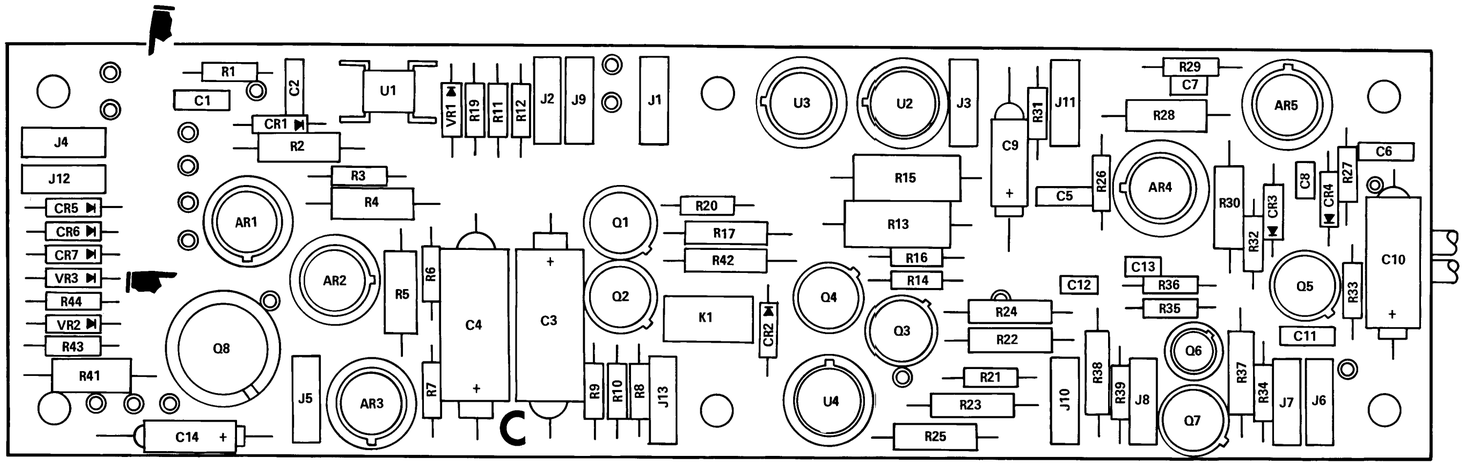

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Figure 3-21. Circuit card assembly 1A2A1 - locational diagram

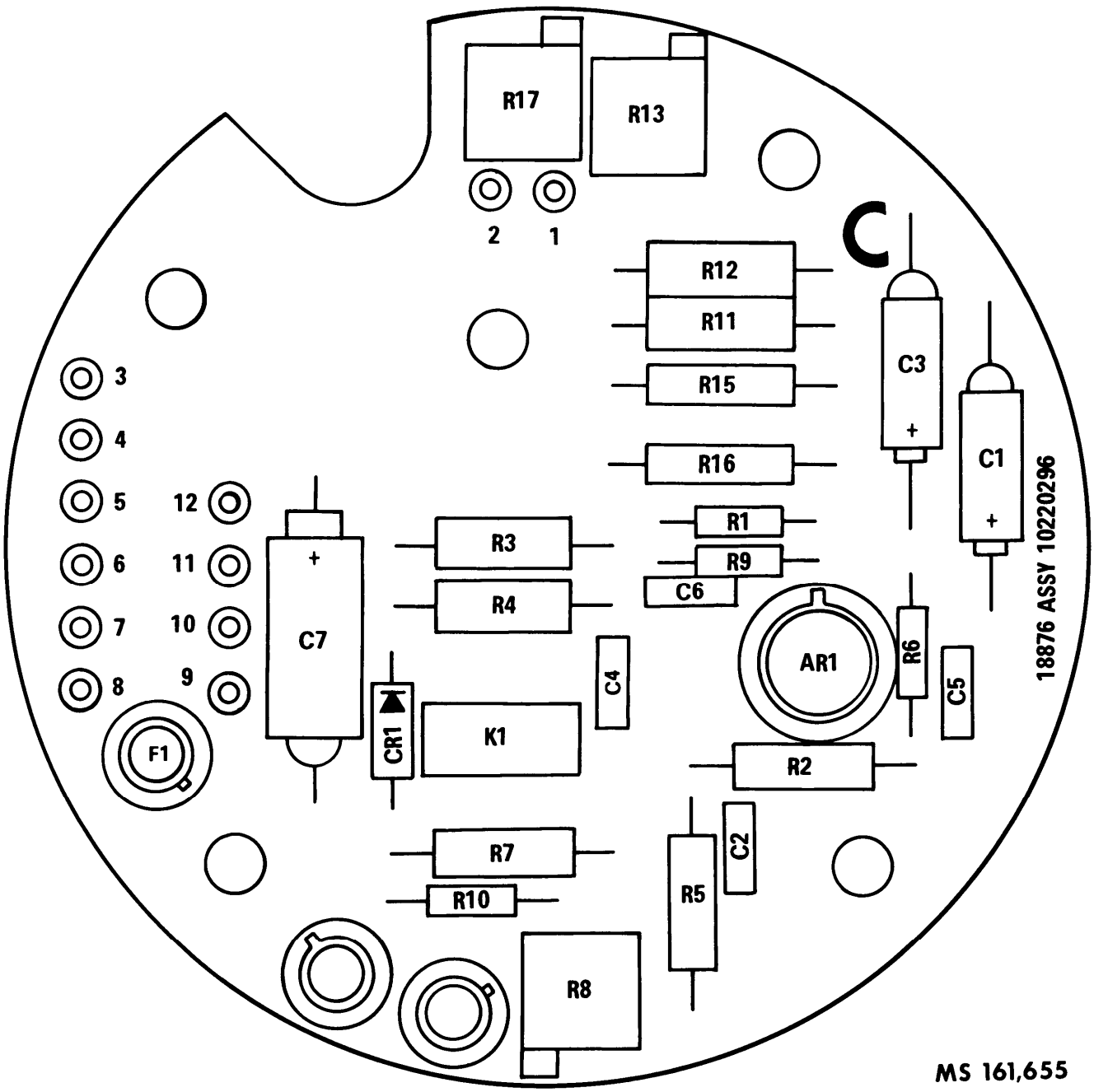

Figure 3-22. Circuit card assembly 3A1 (10220296) - locational diagram

CHAPTER 4
CORRECTIVE MAINTENANCE

4-1. General.

This chapter contains data necessary for direct and general support maintenance of the components of the TTS. This data include alignment, adjustment, removal and installation, disassembly, repair, and assembly instructions pertinent to the TTS .

a. In most cases, removal and replacement is obvious by illustration (refer to TM 9-4935-480-34P for illustrations). The only exception to this for the TTS is the disassembly and assembly of mechanical parts on the OAF. These procedures are contained in paragraph 4-2 and 4-3.

b. Cleaning, inspection, and general testing procedures are contained in TM 9-4935-480-14.

c. Following repair and/or replacement of any items of the TTS which affect operation, the repaired item will be tested, aligned, and adjusted in accordance with procedures contained in TM 9-4935-481-14-1.

d. A list of maintenance materials used to repair the TTS is contained in TM 9-4935-481-14-2.

CAUTION

Do not touch the lens of the tetrahedral prism.

4-2. Disassembly of OAF, Base (fig. 4-1).

a. Remove thumbscrew (1) and washers (2, 3) from mount (4). Remove three screws (5), washers (6) and the mount. Remove nut (7), lockwasher (8), washer (9), and bearings (10) from housing (11) and shaft (12). Remove the shaft. Remove four screws (13), washers (14, 15), seal (16), and the housing from the base (17).

b. Remove retainer (18), stud (19), and washer (20) from the base.

c. Loosen two setscrews (21) and remove the knob (22).

d. Remove pin (23), collar (24), and washer (25). Remove two screws (26), washers (27, 28), housing (29), bearing (30), and two nuts (31). Remove two screws (32), washers (33, 34), and control (35).

e. Remove four screws (36), washers (37, 38), housing (39), and gasket (40)

from the control.

f. Remove shaft (41), two seals (42), and bearings (43) from the housing (39).

g. Remove two pins (44), guide (45), retainer (46), one-half of mitre gear set (47), post (48), shaft (49), seal (50), and bearing (51).

h. Remove shaft (52), seal (53), and bearing (54).

i. Remove remaining half of mitre gear set (47), pin (55), collar (56), shaft (57), seal (58), and bearing (59).

j. Remove plate (60) (using a pocket knife) and bearing (61).

4-3. Assembly of OAF Base (fig. 4-1).

NOTE

Seals are installed by placing the side with the largest metal flange inward.

a. Install plate (60) using cement MMM-A-132 TY2. Position squarely over hole 1.12 inches from outer end and 0.18 inches from the edge of the control. Remove excess cement.

b. Install bearing (61) in control (35). Apply grease MIL-G-10924 to threads of shaft (49) and assemble to post (48). Apply sealing compound MIL-S-22473-C to threads of retainer (46) and guide (45). Install the retainer on the post and turn down to allow installation of the guide to its full depth of threads on the post. Turn the retainer back to a position flush against the guide. Remove excess sealing compound. Install bearing (51) and seal (50) on the shaft. Insert the assembled parts through the top of the control. Install one half of mitre gear set (47), using pin (44). Install seal (58), shaft (57), bearing (59), collar (56), and remaining half of mitre gear set (47). Secure the collar with pin (55) and the gear with pin (44). Apply sufficient quantity of lubricating grease MIL-G-10924 to the gear set.

c. Install bearing (54), seal (53), and shaft (52).

d. Install gasket (40) and housing (39), using four screws (36) and washers (38, 37). Install two bearings (43) flush with face of counterbore. Install two seals (42) and shaft (41).

e. Position control (35) in base (17) and install, using four screws (32) and washers (33 and 34).

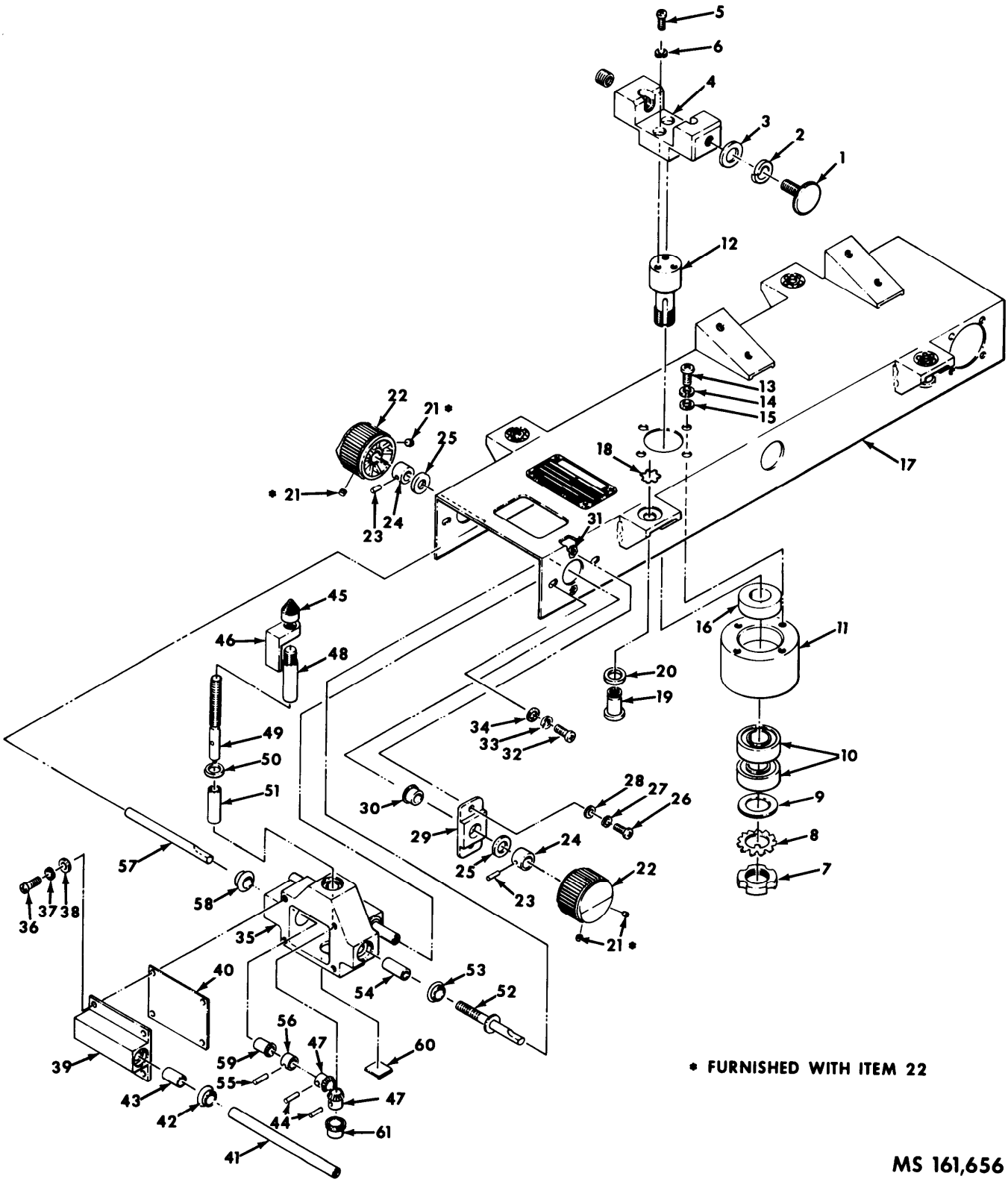

Figure 4-1. Optical alignment fixture base (10278309) disassembly and assembly

f. Install bearing (30) in housing (29). Install housing, using two screws (26) and washers (27, 28), and secure to captive nut (31) located in the base.

g. Install washer (25) and collar (24), using pin (23). Install knob (22).

h. Install washer (20), stud (19), and retainer (18).

i. Install seal (16) with spring side inward into housing (11). Apply sealing compound MIL-S-22473-CV to the surface of the housing that mates with the base and install the housing, using four screws (13) and washers (14 and 15). Remove excess sealant.

j. Apply a small amount of grease MIL-G-10924 to the bearing (10), and apply sealing compound MIL-S-22473-A to the outer diameter only of the bearings. Install shaft (12) and bearings (10) with the stamped faces of the outer races adjacent and secure to the housing with washer (9), lockwasher (8), and nut (7).

k. Engage tang of lockwasher (8) in nearest slot of locknut (7) after torquing locknut to 50 to 60 inch-pounds.

l. Assemble thumbscrew (1) and washers (2, 3) to mount (4). Deform threads on the end of the thumbscrew to retain all hardware. Install the mount to shaft (12), using three screws (5) and washers (6).

4-4. Removal of CRl (fig. 4-2).

a. Remove and retain four screws (1) and eight washers (2) from rear cover of OAC. Remove the cover of the OAC (3). Remove and retain two posts (4) securing 3A1 assembly (5) to OAC. Carefully lift and bend 3A1 assembly up and away from the OAC. (Note: The wire harness prevents total removal).

b. Desolder two thermistor (6) wires (7) from terminals E7 and E8. Identify, tag, and desolder two wires (8) from CR1. Identify, tag, and desolder wire (9) from CR1 (silver tab)(16).

c. Remove nut (10) and thermistor (6) from CR1. (Note: Retain thermistor as spare).

9/64 allen wrench in cap screw (12) and CAREFULLY pry assembly in all directions to break epoxy bond (17). Remove CR1 (13) and beam splitter assembly (14) from OAC.

CAUTION

DO NOT TOUCH surfaces of prism on beam splitter assembly with fingers during this procedure.

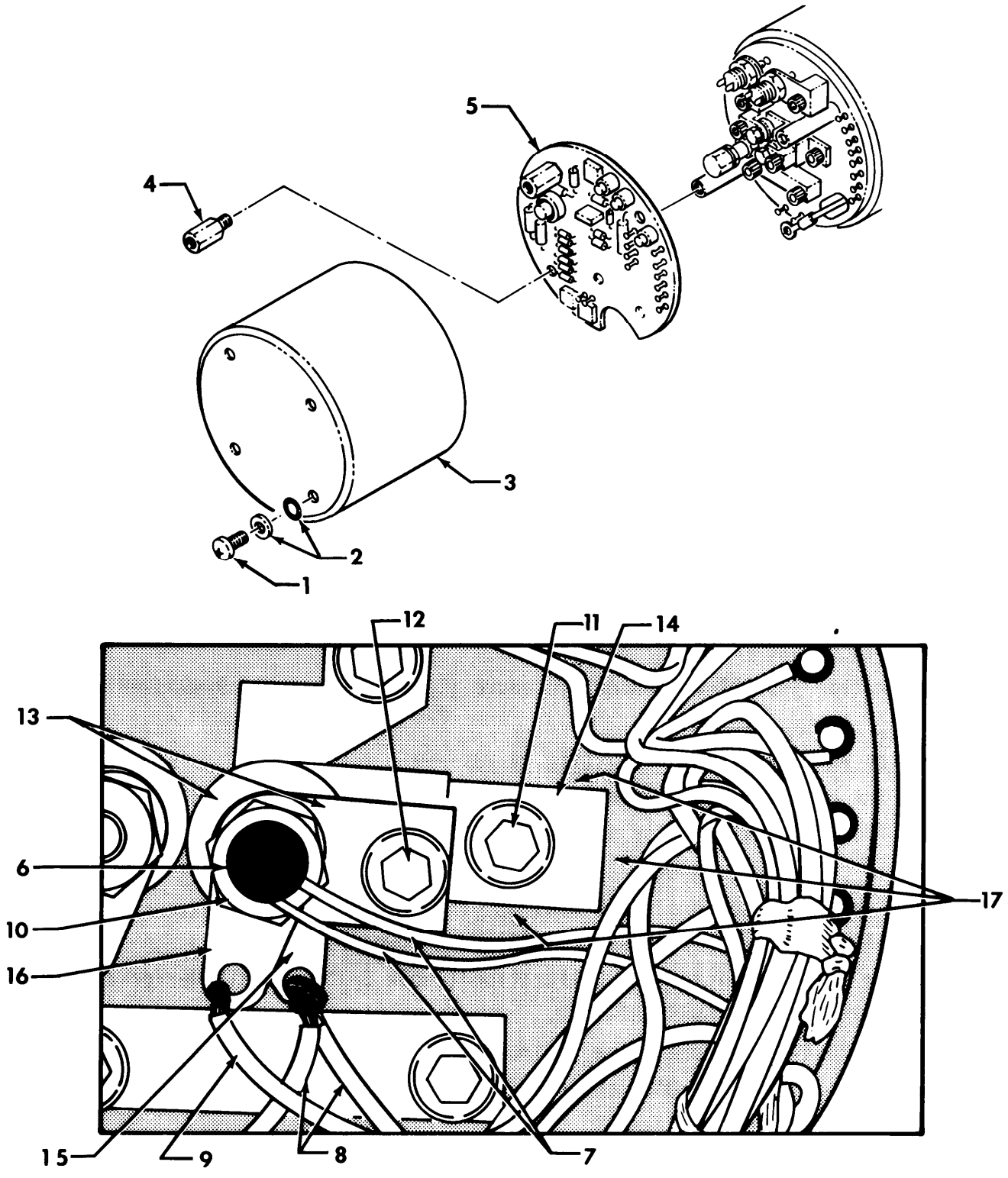

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Figure 4-2. OAC (10220300) - CRI removal and replacement

d. Remove and retain cap screw (12) and separate CR1 (13) and beam splitter assembly (14). Retain beam splitter assembly.

e. Clean residual epoxy from OAC and beam splitter assembly (14) with MEK TT-M-261. Clean beam splitter prism with lens tissue and denatured alcohol. Draw lens tissue across the prism in one direction only. Clean the glass end of the new IR diode with lens tissue and denatured alcohol. Use the end of a cotton swab covered with lens tissue and gently rotate the swab in one direction only. Clean condensor lens on OAC with lens tissue, swab, and denatured alcohol as above.

4-5. Replacement of CR1 (fig. 4-2).

a. Mount beam splitter assembly (14) on OAC using cap screw (11). Do not torque cap screw, but tighten sufficiently to prevent movement. Mount the new CR1 on beam splitter assembly (14), using cap screw (12), positioning the cathode tab (gold) (15) straight downward. Torque cap screw (12) to 11.0 ±1.O inch pounds.

b. Solder the thermistor wires (7) to terminals E7 and E8. Solder two wires (8) to the cathode tab (15) or CR1. Solder wire (9) to CR1 (silver tab)(16).

c. Loosen nut (10) to allow rotation of CR1. If thermistor breaks off, retain for later replacement.

d. Perform the TTS CR1 alignment procedure (Table 2-61) in TM 9-4935-481-40.

4-6. Bonding Requirements for CR1 (fig. 4-2).

a. Bond the beam splitter assembly (14) at the junction (17) using adhesive MIL-A-14042. Bond the thermistor to the nut (10) using conductive adhesive MPD 9148.

b. Allow adhesives to cure for a minimum of 90 minutes.

c. Carefully secure the 3A1 assembly (5) using two posts (4).

d. Perform the TTS Maintenance Calibration (Table 3-13) and TTS Performance Test (Table 3-14) in TM 9-4935-481-14-1.

e. Allow adhesives to cure for a minimum of 24 hours.

f. Replace rear cover of OAC, securing with four screws (1) and eight washers (2).

4-7. Removal of CR2 (fig. 4-3).

a. Perform operations in paragraph 4-4 a.

b. Identify, tag, and desolder wire (1) from CR2 (silver tab) (2). Identify,

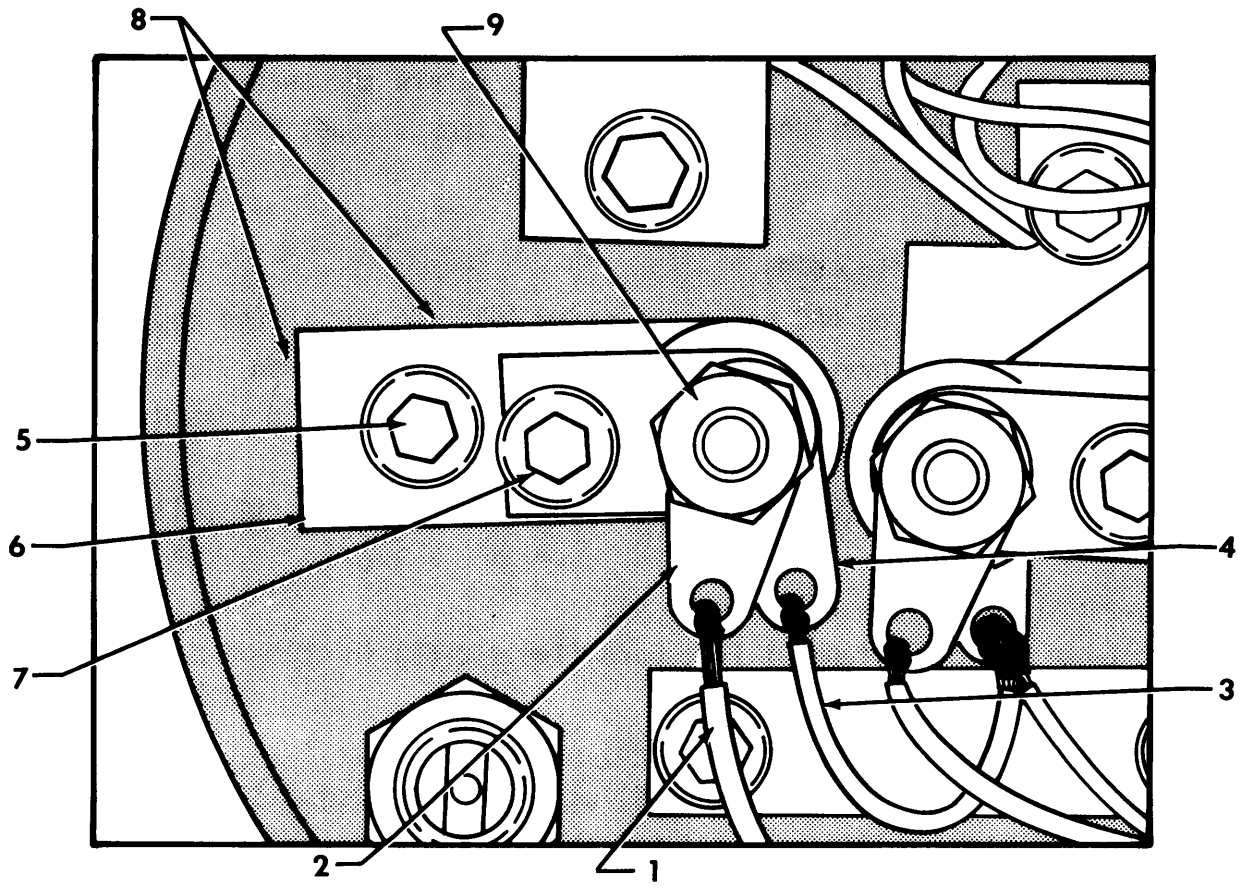

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Figure 4-3. OAC (10220300) - CR2 removal and replacement

tag, and desolder wire (3) from CR2 (gold tab) (4). Remove and retain cap screw (5) from plate (6). Insert a 9/64 allen wrench in cap screw (7) and carefully pry assembly in all directions to break epoxy bond (8). Remove CR2 and plate (6) from OAC,

c. Remove and retain cap screw (7) and separate CR2 and plate (6). Retain plate.

d. Clean residual epoxy from OAC and plate (6) with MEK TT-M-261. Clean the glass end of the new IR diode with lens tissue and denatured alcohol. Use the end of a cotton swab covered with lens tissue and gently rotate the swab in one direction only. Clean the condensor lens of the OAC with lens tissue, swab, and denatured alcohol as above.

4-8. Replacement of CR2 (fig. 4-3).

a. Secure the plate (6) on OAC using cap screw (5). Do not torque cap screw, but tighten sufficiently to prevent movement. Secure the new CR2 on plate (6) using cap screw (7), position the cathode (gold tab) (4) straight downward. Torque cap screw (7) to 11.0 ±1.O inch pounds.

b. Solder wire (3) to CR2 (gold tab) (4). Solder wire (1) to CR2 (silver tab) (2).

c. Loosen nut (9) to allow rotation of CR2.

d. Perform the TTS CR2 Alignment Procedure (Table 2-62) in TM 9-4935-482-40.

4-9. Bonding Requirements for CR2 (fig. 4-3).

a. Bond the plate (6) at the junction (8) using adhesive MIL-A-14042.

b. Perform operations in paragraphs 4-6 b. through 4-6 f.

4-10. Removal of CR3 (fig. 4-4).

a. Perform operations in paragraph 4-4 a.

b. Remove and retain two screws (1) and washers (2). Remove CR3 and transistor socket (4) from bracket (5).

c. Observe CR3's polarity, and remove CR3 (3) from transistor socket (4).

4-11. Replacement of CR3 (fig. 4-4).

a. Install new CR3 (3), noting polarity, in transistor socket (4). Using two

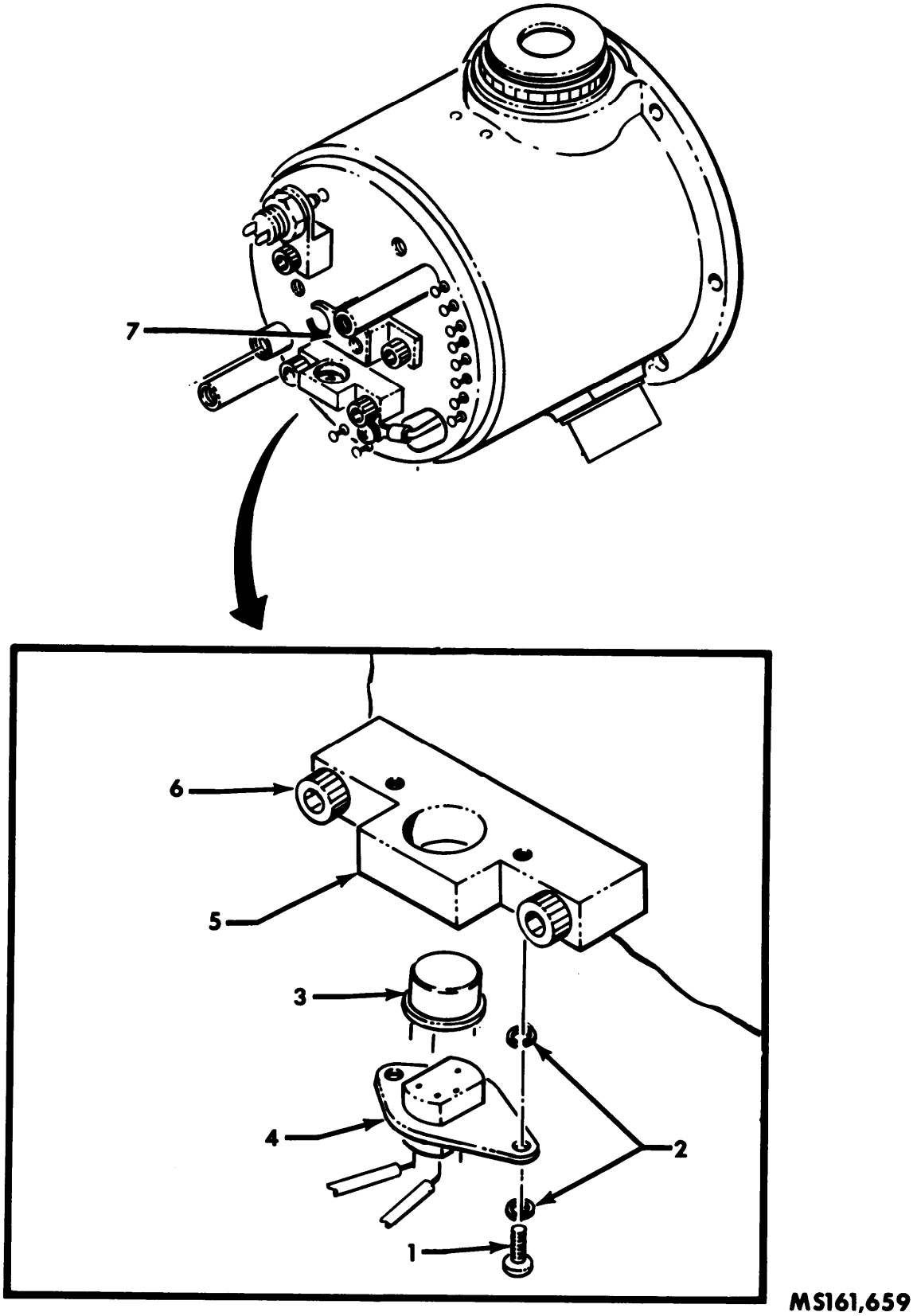

Figure 4-4. OAC (10220300) - CR3 removal and replacement

screws (1) and washers (2), secure CR3 and socket to bracket (5).

b. Perform the TTS CR3 Alignment Procedure (Table 2-63) in TM 9-4935-48240.

4-12. Removal of DSl (fig. 4-5).

a. Perform operations in paragraph 4-4 a.

b. Remove cap screw (1) and mounting block (2) from OAC. Remove failed DS1 (4) from socket (5) by removing bushing (3).

4-13. Replacement of DS1 (fig. 4-5).

a. Insert new DS1 into socket (5) and install bushing (3). Install mounting block (2) on OAC with cap screw (l), positioning DS1 in direct contact with red lens. Torque cap screw to 11.0 ±1.0 inch pounds.

b. Carefully secure 3A1 assembly, using two posts removed in 4-4 a. Replace rear cover of OAC, securing with four screws and eight washers removed in 4-4 a.

4-14. Removal of DS2 (fig. 4-6).

a. Perform operations in paragraph 4-4 a.

b. Remove cap screw (1) and mounting block (2) from OAC. Remove failed DS2 (3) from socket (4) by removing bushing (5).

4-15. Replacement of DS2 (fig. 4-6).

a. Insert new DS2 into socket (4) and install bushing (5). Install mounting block (2) on OAC with cap screw (l), positioning DS2 over and in line with aperature. Torque cap screw to 11.0 ± 1.0 inch pounds.

c. Carefully secure 3A1 assembly, using two posts removed in 4-4 a. Replace rear cover of OAC, securing with four screws and eight washers removed in 4-4 a.

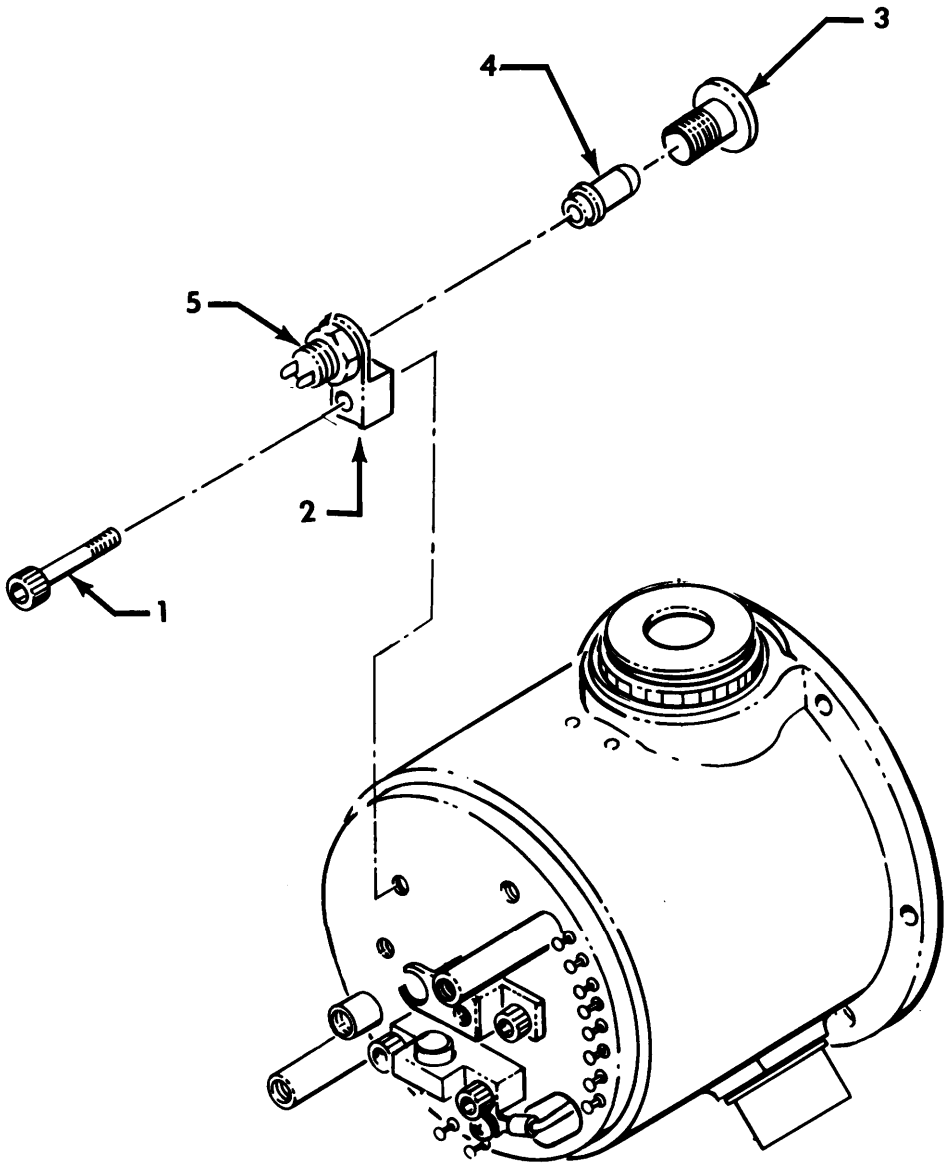

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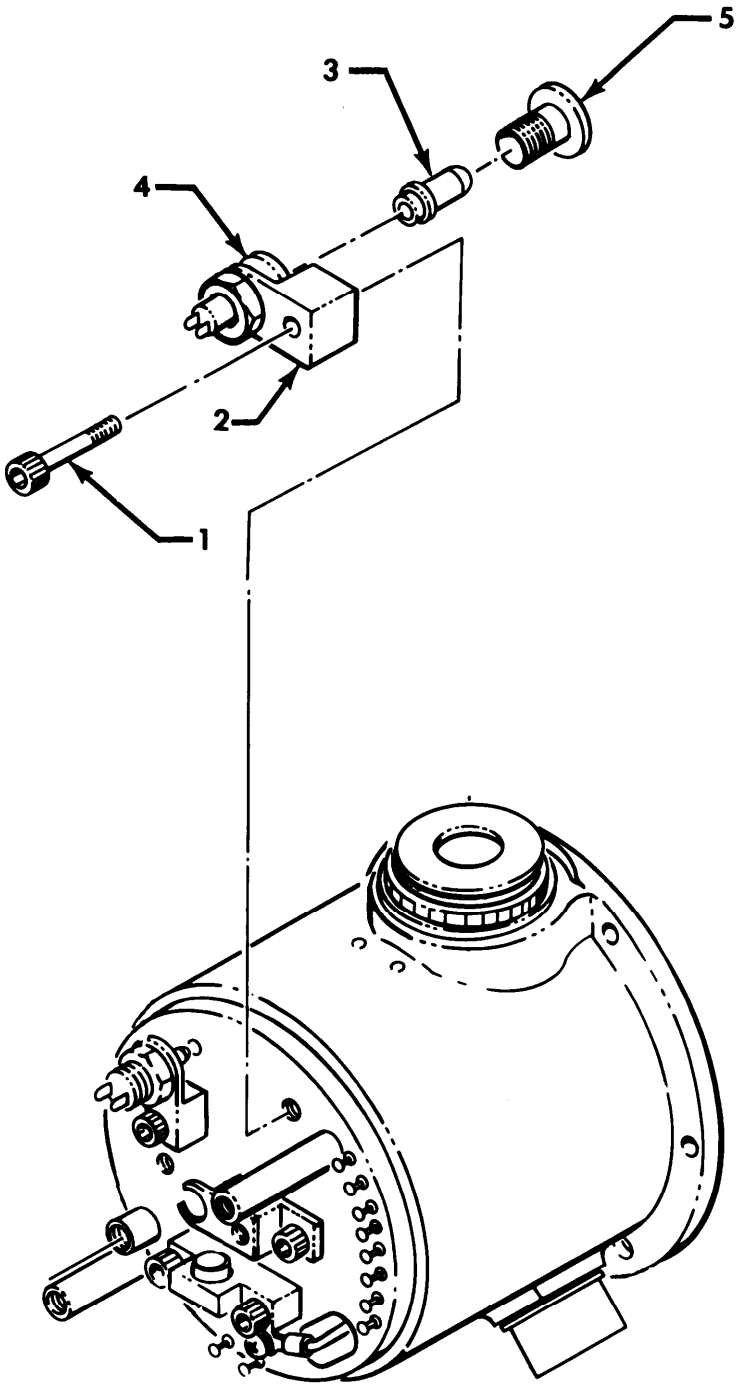
Figure 4-5. OAC (10220300) - DSI removal and replacement



MS161,661

Figure 4-6. OAC (10220300) - DS2 removal and replacement

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Official:

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21-2	step 1C		21-2	Reads: Multimeter B indicates 600 K ohms to 9000 K ohms. Change to read: Multimeter B indicates 600 K ohms minimum. Reason: Circuit being checked could measure infinity. Multimeter can read above 9000 K ohms and still be correct.

SAMPLE

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U.S. Army Missile Command
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Redstone Arsenal, AL 35898-5238

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THE METRIC SYSTEM AND EQUIVALENTS

'NEAR MEASURE

. Centimeter = 10 Millimeters = 0.01 Meters = 0.3937 Inches
1 Meter = 100 Centimeters = 1000 Millimeters = 39.37 Inches
1 Kilometer = 1000 Meters = 0.621 Miles

'VEIGHTS

Gram = 0.001 Kilograms = 1000 Milligrams = 0.035 Ounces
1 Kilogram = 1000 Grams = 2.2 lb.
1 Metric Ton = 1000 Kilograms = 1 Megagram = 1.1 Short Tons

LIQUID MEASURE

1 Milliliter = 0.001 Liters = 0.0338 Fluid Ounces
1 Liter = 1000 Milliliters = 33.82 Fluid Ounces

SQUARE MEASURE

1 Sq. Centimeter = 100 Sq. Millimeters = 0.155 Sq. Inches
1 Sq. Meter = 10,000 Sq. Centimeters = 10.76 Sq. Feet
1 Sq. Kilometer = 1,000,000 Sq. Meters = 0.386 Sq. Miles

CUBIC MEASURE

1 Cu. Centimeter = 1000 Cu. Millimeters = 0.06 Cu. Inches
1 Cu. Meter = 1,000,000 Cu. Centimeters = 35.31 Cu. Feet

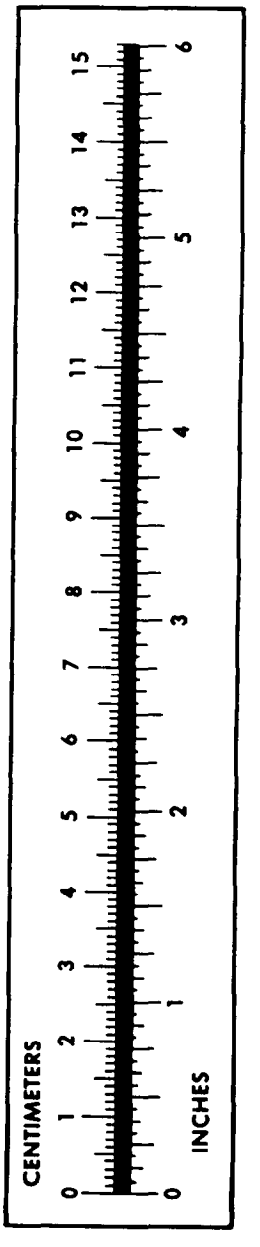
TEMPERATURE

5/9(°F - 32) = °C
212° Fahrenheit is evuivalent to 100° Celsius
90° Fahrenheit is equivalent to 32.2° Celsius
32° Fahrenheit is equivalent to 0° Celsius
9/5C° + 32 =°F

APPROXIMATE CONVERSION FACTORS

TO CHANGE	TO	MULTIPLY BY
Inches	Centimeters	2.540
Feet	Meters	0.305
Yards	Meters	0.914
Miles	Kilometers	1.609
Square Inches	Square Centimeters	6.451
Square Feet	Square Meters	0.093
Square Yards	Square Meters	0.836
Square Miles	Square Kilometers	2.590
Acres	Square Hectometers	0.405
Cubic Feet	Cubic Meters	0.028
Cubic Yards	Cubic Meters	0.765
Fluid Ounces	Milliliters	29.573
ıts	Liters	0.473
arts	Liters	0.946
allons	Liters	3.785
Ounces	Grams	28.349
Pounds	Kilograms	0.454
Short Tons	Metric Tons	0.907
Pound-Feet	Newton-Meters	1.356
Pounds per Square Inch	Kilopascals	6.895
Miles per Gallon	Kilometers per Liter	0.425
Miles per Hour	Kilometers per Hour	1.609

TO CHANGE	TO	MULTIPLY BY
Centimeters	Inches	0.394
Meters	Feet	3.280
Meters	Yards	1.094
Kilometers	Miles	0.621
Square Centimeters	Square Inches	0.155
Square Meters	Square Feet	10.764
Square Meters	Square Yards	1.196
Square Kilometers	Square Miles	0.386
Square Hectometers	Acres	2.471
Cubic Meters	Cubic Feet	35.315
Cubic Meters	Cubic Yards	1.308
Milliliters	Fluid Ounces	0.034
Liters	Pints	2.113
Liters	Quarts	1.057
ers	Gallons	0.264
ms	Ounces	0.035
ograms	Pounds	2.205
Metric Tons	Short Tons	1.102
Newton-Meters	Pounds-Feet	0.738
Kilopascals	Pounds per Square Inch	0.145
lometers per Liter	Miles per Gallon	2.354
meters per Hour	Miles per Hour	0.621



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